19-3583; Rev 1; 6/05

0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers

General Description

The MAX5060/MAX5061 pulse-width modulation (PWM) DC-DC controllers provide high-output-current capability in a compact package with a minimum number of external components. These devices utilize an average-current-mode control that enables optimal use of low $R_{DS(ON)}$ MOSFETs, eliminating the need for external heatsinks even when delivering high output currents.

Differential sensing (MAX5060) enables accurate control of the output voltage, while adaptive voltage positioning provides optimum transient response. An internal regulator enables operation with 4.75V to 5.5V or 7V to 28V input voltage ranges. The high switching frequency, up to 1.5MHz, allows the use of low-output inductor values and input capacitor values. This accommodates the use of PC-board-embedded planar magnetics.

The MAX5060 features a clock output with 180° phase delay to control a second out-of-phase converter for lower capacitor ripple currents. The MAX5060 also limits the reverse current if the bus voltage becomes higher than the regulated output voltage. The MAX5060 is specifically designed to limit current sinking when multiple power-supply modules are paralleled. The MAX5060/MAX5061 offer an adjustable 0.6V to 5.5V output voltage. The MAX5060 offers an overvoltage protection, power-good signal, and an output enable function.

The MAX5060/MAX5061 operate over the automotive temperature range (-40°C to +125°C). The MAX5060 is available in a 28-pin thin QFN package while the MAX5061 is available in a 16-pin TSSOP package.

Applications

Servers and Workstations

Point-of-Load Telecom DC-DC Regulators

Networking Systems

RAID Systems

High-End Desktop Computers

Selector Guide

PART	OUTPUT
MAX5060	Average-Current-Mode DC-DC Controller for 5V/12V/24V Input Bus with CLKOUT, Load Monitoring, Overvoltage, EN Input, SYNC Input, and PGOOD Output
MAX5061	Average-Current-Mode DC-DC Controller for 5V/12V/24V Input with SYNC/ENABLE Input

Features

- ♦ **4.75V to 5.5V or 7V to 28V Input Voltage Range**
- ♦ **Adjustable Output Voltage from 0.6V to 5.5V**
- ♦ **Up to 30A Output Current**
- ♦ **Can Parallel Outputs For Higher Output Current**
- ♦ **Programmable Adaptive Output Voltage Positioning**
- ♦ **True-Differential Remote Output Sensing (MAX5060)**
- ♦ **Average-Current-Mode Control**
  - **Superior Current Sharing Between Paralleled Modules**
  - **Accurate Current Limit Eliminates MOSFET and Inductor Derating**
- ♦ **Limits Reverse Current Sinking in Paralleled Modules (MAX5060)**
- ♦ **Programmable Switching Frequency from 125kHz to 1.5MHz**
- ♦ **Integrated 4A Gate Drivers**
- ♦ **Clock Output for 180° Out-of-Phase Operation (MAX5060)**
- ♦ **Voltage Signal Proportional to Output Current for Load Monitoring (MAX5060)**
- ♦ **Output Overvoltage Crowbar Protection (MAX5060)**
- ♦ **Programmable Hiccup Current-Limit Threshold and Response Time**
- ♦ **Overtemperature Thermal Shutdown**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5060ATI	-40°C to +125°C	28 TQFN-EP*
MAX5060ETI	-40°C to +85°C	28 TQFN-EP*
MAX5061AUE	-40°C to +125°C	16 TSSOP-EP*
MAX5061EUE	-40°C to +85°C	16 TSSOP-EP*

**EP = Exposed pad.*

Pin Configurations appear at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

IN to SGND ....-0.3V to +30V
BST to SGND ....-0.3V to +35V
DH to LX ....-0.3V to [(V_{BST} - $V_{LX\_}$) + 0.3V]
DL to PGND (MAX5060) ....-0.3V to (V_{DD} + 0.3V)
DL to PGND (MAX5061) ....-0.3V to (V_{CC} + 0.3V)
BST to LX ....-0.3V to +6V
V_{CC} to SGND ....-0.3V to +6V
V_{CC}, V_{DD} to PGND ....-0.3V to +6V
SGND to PGND ....-0.3V to +0.3V
Current Sink in PGOOD 6mA

All Other Pins to SGND ....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 21.3mW/°C above +70°C)* 1702mW
28-Pin TQFN (derate 34.5mW/°C above +70°C)* 2758mW
Operating Temperature Range
MAX5060A_ _ and MAX5061A_ _ ....-40°C to +125°C
MAX5060E_ _ and MAX5061E_ _ ....-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

**Per JEDEC 51 standard.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{DD} = V_{CC} (MAX5060 only), T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input Voltage Range	V_{IN}		7		28	V
		Short IN and V_{CC} together for 5V input operation	4.75		5.50	
Quiescent Supply Current	I_Q	EN = V_{CC} or SGND, not switching		2.7	5.5	mA
Efficiency	η	I_{LOAD} = 20A, V_{IN} = 12V, V_{OUT} = 3.3V		90		%
OUTPUT VOLTAGE						
SENSE+ to SENSE- Accuracy (MAX5060) (Note 2)		No load, V_{CC} = 4.75V to 5.5V, f_{SW} = 500kHz	0.594	0.6	0.606	V
		No load, V_{IN} = 7V to 28V, f_{SW} = 500kHz	0.594	0.6	0.606	
Soft-Start Time	t_{SS}			1024		Clock Cycles
EAN Reference Voltage (MAX5061)	V_{REF}	No load, V_{CC} = 4.75V to 5.5V, no switching	0.591	0.6	0.606	V
		No load, V_{IN} = 7V to 28V, no switching	0.591	0.6	0.606	
STARTUP/INTERNAL REGULATOR						
V_{CC} Undervoltage Lockout	UVLO	V_{CC} rising	4.1	4.3	4.5	V
V_{CC} Undervoltage Lockout Hysteresis				200		mV
V_{CC} Output Voltage		V_{IN} = 7V to 28V, I_{SOURCE} = 0 to 60mA	4.85	5.1	5.30	V
MOSFET DRIVERS						
Output-Driver Impedance	R_{ON}	Low or high output, $I_{SOURCE/SINK}$ = 20mA		1.1	3	Ω
Output-Driver Source/Sink Current	$I_{DH\_}$, $I_{DL\_}$			4		A
Nonoverlap Time	t_{NO}	$C_{DH/DL}$ = 5nF		35		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{DD} = V_{CC} (MAX5060 only), T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Switching Frequency Range			125		1500	kHz
Switching Frequency	f_{SW}	R_T = 500kΩ	121	125	129	kHz
		R_T = 120kΩ	495	521	547	
		R_T = 39.9kΩ	1515	1620	1725	
Switching Frequency Accuracy		120kΩ ≤ R_T ≤ 500kΩ	-5		+5	%
		40kΩ ≤ R_T ≤ 120kΩ	-8		+8	
CLKOUT Phase Shift (MAX5060)	ϕ_{CLKOUT}	f_{SW} = 125kHz		180		degrees
CLKOUT Output Low Level (MAX5060)	$V_{CLKOUTL}$	I_{SINK} = 2mA			0.4	V
CLKOUT Output High Level (MAX5060)	$V_{CLKOUTH}$	I_{SOURCE} = 2mA	4.5			V
SYNC Input-High Pulse Width	t_{SYNC}	RT/SYNC (MAX5060), RT/SYNC/EN (MAX5061)	200			ns
SYNC Input Clock High Threshold	V_{SYNCH}	RT/SYNC (MAX5060), RT/SYNC/EN (MAX5061)	2.0			V
SYNC Input Clock Low Threshold	V_{SYNCL}	RT/SYNC (MAX5060), RT/SYNC/EN (MAX5061)			0.4	V
SYNC Pullup Current	I_{SYNC_OUT}	$V_{RT/SYNC}$ = 0V (MAX5060), $V_{RT/SYNC/EN}$ = 0V (MAX5061)		250	750	µA
SYNC Power-Off Level	V_{SYNC_OFF}				0.4	V
CURRENT LIMIT						
Average Current-Limit Threshold	V_{CL}	CSP to CSN	24.0	26.9	28.2	mV
Reverse Current-Limit Threshold	V_{CLR}	CSP to CSN (MAX5060)	-3.2	-2.3	-0.1	mV
Cycle-by-Cycle Current Limit		CSP to CSN		60		mV
Cycle-by-Cycle Overload Response Time		V_{CSP} to V_{CSN} = 75mV		260		ns
Hiccup Divider Ratio		LIM to V_{CM}, no switching	0.547	0.558	0.565	V/V
Hiccup Reset Delay				200		ms
LIM Input Impedance		LIM to SGND		55.9		kΩ
CURRENT-SENSE AMPLIFIER						
CSP to CSN Input Resistance	R_{CS}			4		kΩ
Common-Mode Range	$V_{CMR(CS)}$	V_{IN} = 7V to 28V	0		5.5	V
Input Offset Voltage	$V_{OS(CS)}$			0.1		mV
Amplifier Gain	$A_{V(CS)}$			34.5		V/V
3dB Bandwidth	f_{3dB}			4		MHz

0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{DD} = V_{CC} (MAX5060 only), T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-ERROR AMPLIFIER (Transconductance Amplifier)						
Transconductance	g_C			550		µS
Open-Loop Gain	$A_{VOL(CE)}$	No load		50		dB
DIFFERENTIAL VOLTAGE AMPLIFIER (DIFF, MAX5060 only)						
Common-Mode Voltage Range	$V_{CMR(DIFF)}$		0		+1.0	V
DIFF Output Voltage	V_{CM}	V_{SENSE+} = V_{SENSE-} = 0V		0.6		V
Input Offset Voltage	$V_{OS(DIFF)}$		-1		+1	mV
Amplifier Gain	$A_{V(DIFF)}$		0.994	1	1.006	V/V
3dB Bandwidth	f_{3dB}	C_{DIFF} = 20pF		3		MHz
Minimum Output-Current Drive	$I_{OUT(DIFF)}$		4			mA
SENSE+ to SENSE- Input Resistance	R_{VS}	V_{SENSE-} = 0V	50	100		kΩ
V_IOUT AMPLIFIER (V_IOUT, MAX5060 only)						
Gain-Bandwidth Product		V_{V_IOUT} = 2.0V		4		MHz
3dB Bandwidth		V_{V_IOUT} = 2.0V		1.0		MHz
Output Sink Current			30			µA
Output Source Current			90			µA
Maximum Load Capacitance				50		pF
V_IOUT Output to I_{OUT} Transfer Function		R_{SENSE} = 1mΩ, 100mV ≤ V_IOUT ≤ 5.5V	132.3	135	137.7	mV/A
Offset Voltage				1		mV
VOLTAGE-ERROR AMPLIFIER (EAOUT)						
Open-Loop Gain	A_{VOLEA}			70		dB
Unity-Gain Bandwidth	f_{GBW}			3		MHz
EAN Input Bias Current	$I_{B(EA)}$	V_{EAN} = 2.0V (MAX5060) V_{EAN} = 0.4V, V_{EAOUT} = GND (MAX5061)	-0.2	0.03	+0.2	µA
Error-Amplifier Output-Clamping Voltage	$V_{CLAMP(EA)}$	With respect to V_{CM} (MAX5060), with respect to SGND (MAX5061)	883	930	976	mV
POWER-GOOD AND OVERVOLTAGE PROTECTION (MAX5060 only)						
PGOOD Trip Level	V_{UV}	PGOOD goes low when V_{OUT} is below this threshold	87.5	90	92.5	$\%V_{OUT}$
PGOOD Output Low Level	V_{PGLO}	I_{SINK} = 4mA			0.4	V
PGOOD Output Leakage Current	I_{PG}	PGOOD = V_{CC}			1	µA
OVI Trip Threshold	OVP_{TH}	With respect to SGND	1.244	1.276	1.308	V
OVI Input Bias Current	I_{OVI}			0.2		µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{DD} = V_{CC} (MAX5060 only), T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE INPUTS						
EN Input High Voltage (MAX5060)	V_{EN}	EN rising	2.437	2.5	2.562	V
EN Input Hysteresis (MAX5060)				0.28		V
EN Pullup Current (MAX5060)	I_{EN}		13.5	15	16.5	µA
RT/SYNC/EN Input High Voltage Enable (MAX5061)	$V_{RT/SYNC/EN\_H}$		1.6			V
RT/SYNC/EN Input Low Voltage Disable (MAX5061)	$V_{RT/SYNC/EN\_L}$				0.4	V
THERMAL SHUTDOWN						
Thermal Shutdown		Temperature rising		+150		°C
Thermal-Shutdown Hysteresis				30		°C

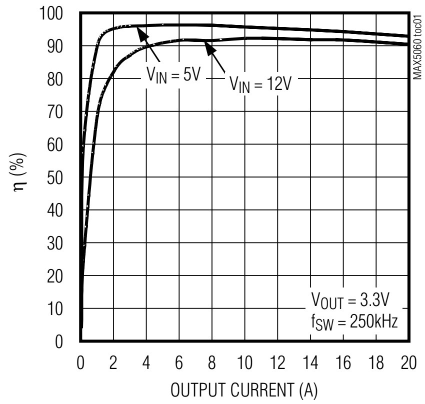
Note 1: Specifications at T_A = +25°C are 100% tested. Specifications over the temperature range are guaranteed by design.
Note 2: Does not include an error due to finite error amplifier gain (see the *Voltage-Error Amplifier* section).

0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers

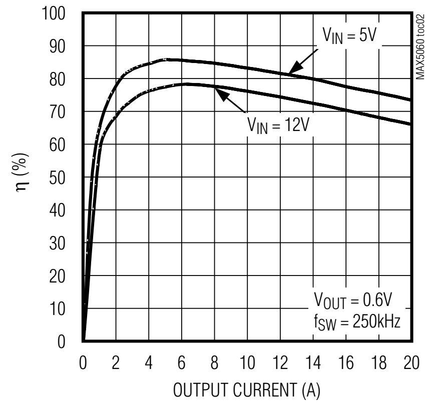
Typical Operating Characteristics

(T_A = +25°C, Figures 1 and 2, unless otherwise noted.)

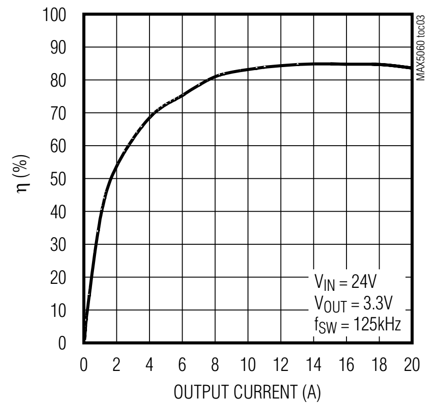
EFFICIENCY vs. OUTPUT CURRENT AND INPUT VOLTAGE



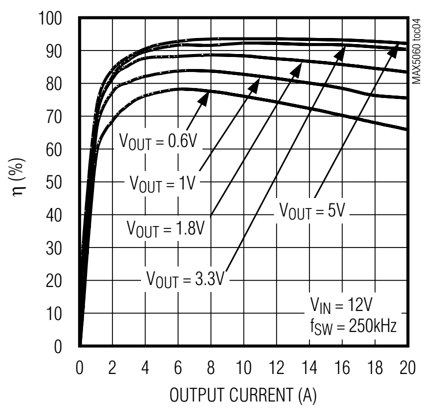
EFFICIENCY vs. OUTPUT CURRENT AND INPUT VOLTAGE



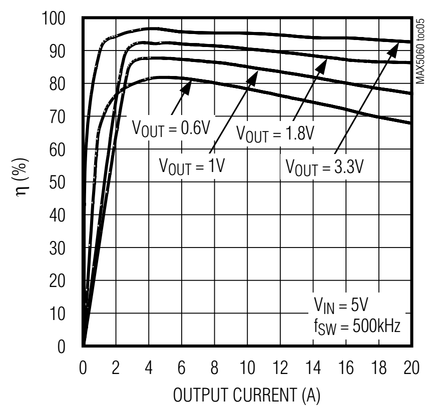
EFFICIENCY vs. OUTPUT CURRENT



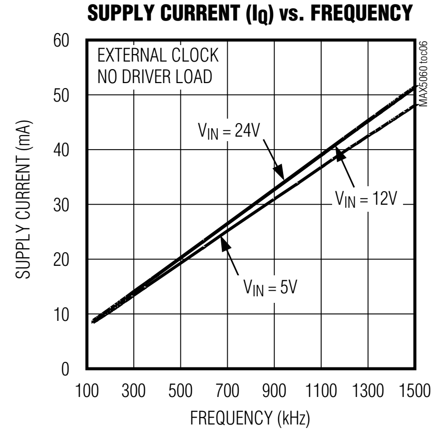
EFFICIENCY vs. OUTPUT CURRENT AND OUTPUT VOLTAGE



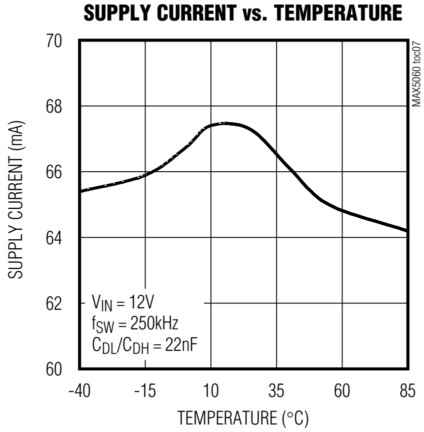
EFFICIENCY vs. OUTPUT CURRENT AND OUTPUT VOLTAGE



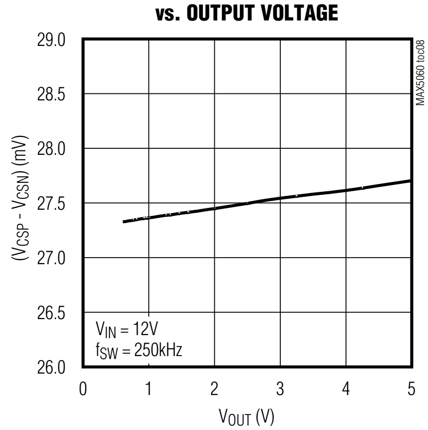
SUPPLY CURRENT (I_Q) vs. FREQUENCY



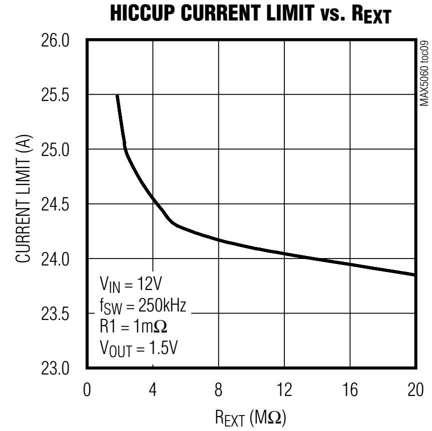
SUPPLY CURRENT vs. TEMPERATURE



CURRENT-SENSE THRESHOLD vs. OUTPUT VOLTAGE



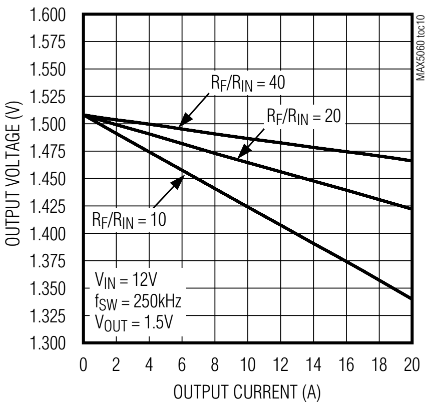
HICCUP CURRENT LIMIT vs. R_{EXT}



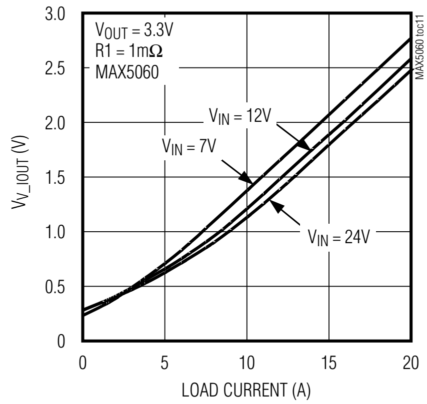
Typical Operating Characteristics (continued)

(T_A = +25°C, Figures 1 and 2, unless otherwise noted.)

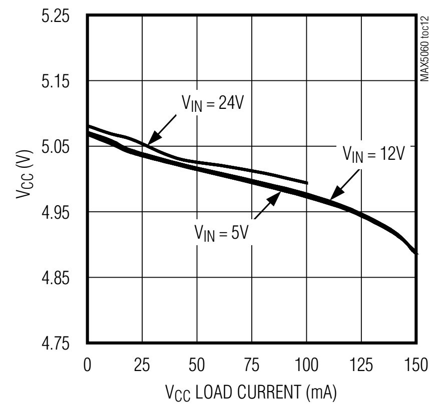
OUTPUT VOLTAGE vs. OUTPUT CURRENT AND ERROR AMPLIFIER GAIN (R_F/R_{IN})



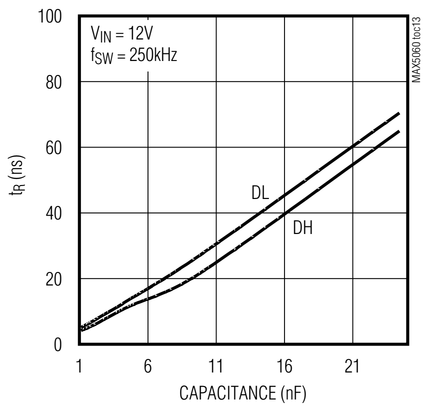
V_IOUT VOLTAGE vs. LOAD CURRENT



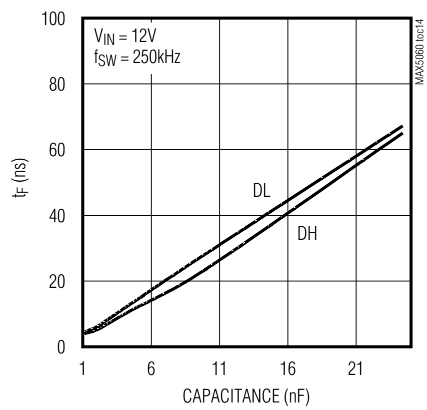
V_{CC} LOAD REGULATION vs. INPUT VOLTAGE



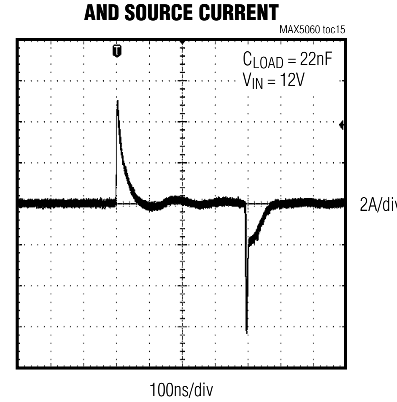
DRIVER RISE TIME vs. DRIVER LOAD CAPACITANCE



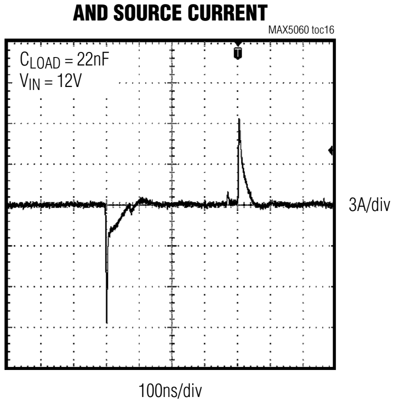
DRIVER FALL TIME vs. DRIVER LOAD CAPACITANCE



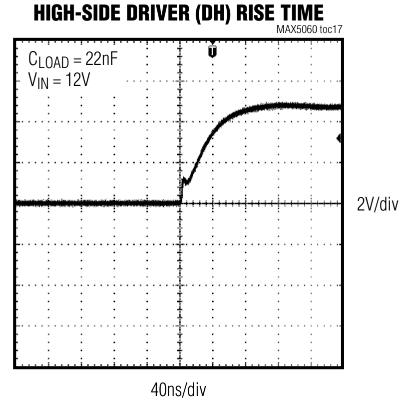
HIGH-SIDE DRIVER (DH) SINK AND SOURCE CURRENT



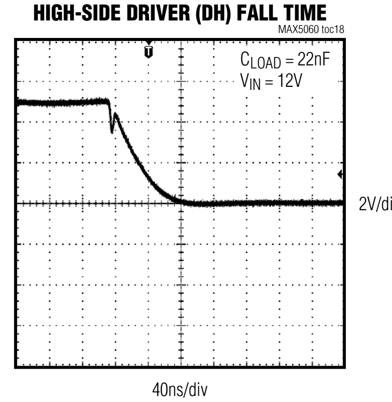
LOW-SIDE DRIVER (DL) SINK AND SOURCE CURRENT



HIGH-SIDE DRIVER (DH) RISE TIME



HIGH-SIDE DRIVER (DH) FALL TIME

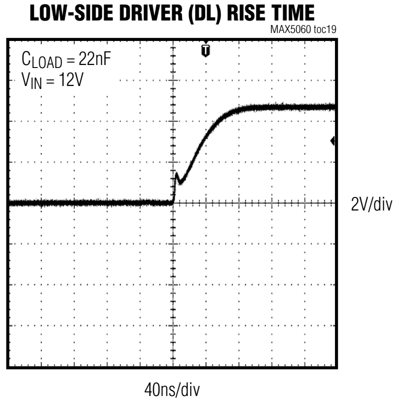


0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers

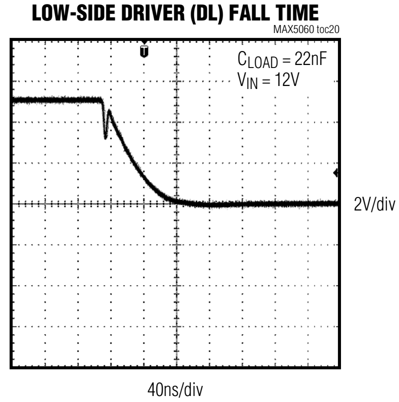
Typical Operating Characteristics (continued)

(T_A = +25°C, Figures 1 and 2, unless otherwise noted.)

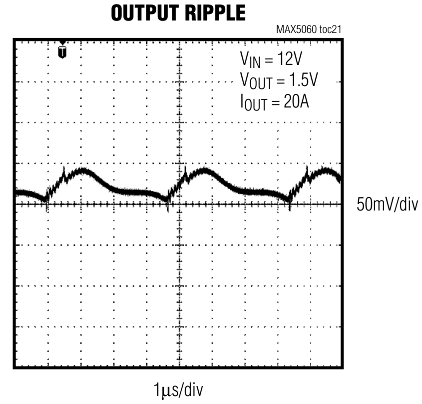
LOW-SIDE DRIVER (DL) RISE TIME



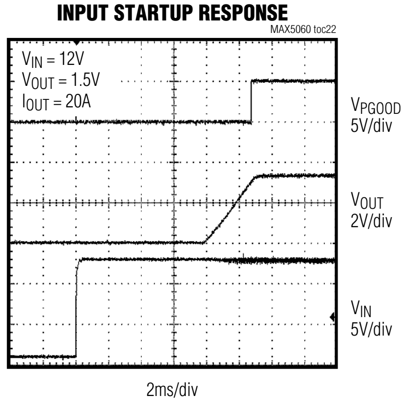
LOW-SIDE DRIVER (DL) FALL TIME



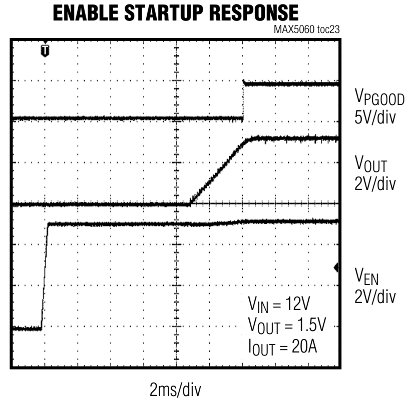
OUTPUT RIPPLE



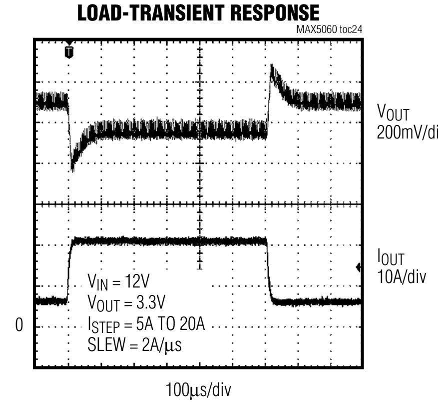
INPUT STARTUP RESPONSE



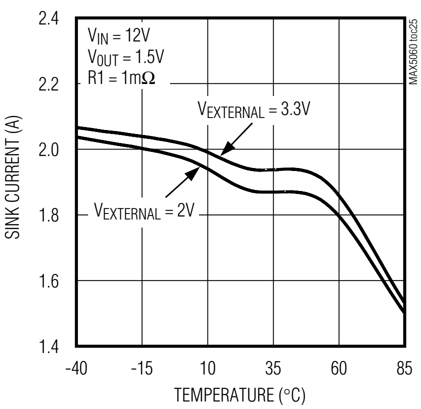
ENABLE STARTUP RESPONSE



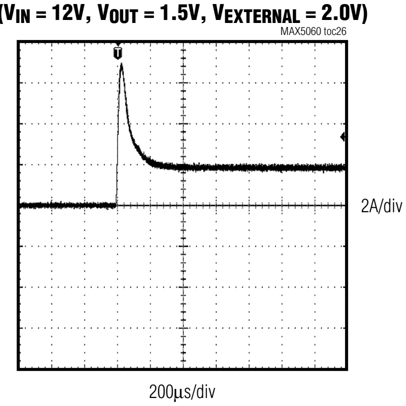
LOAD-TRANSIENT RESPONSE



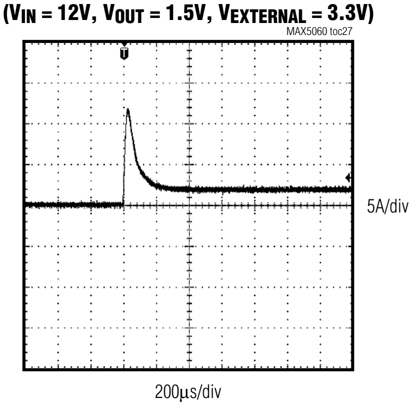
REVERSE CURRENT SINK vs. TEMPERATURE



REVERSE CURRENT SINK AT INPUT TURN-ON (V_{IN} = 12V, V_{OUT} = 1.5V, $V_{EXTERNAL}$ = 2.0V)

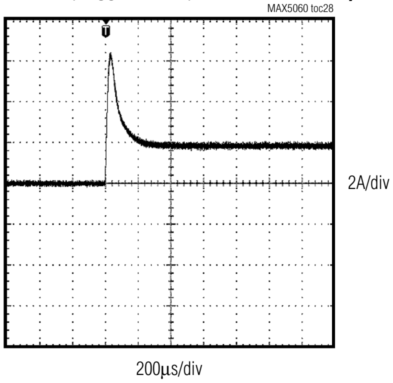


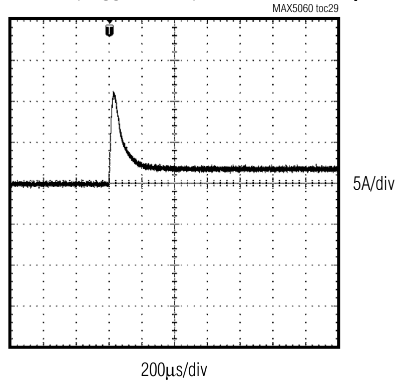
REVERSE CURRENT SINK AT INPUT TURN-ON (V_{IN} = 12V, V_{OUT} = 1.5V, $V_{EXTERNAL}$ = 3.3V)

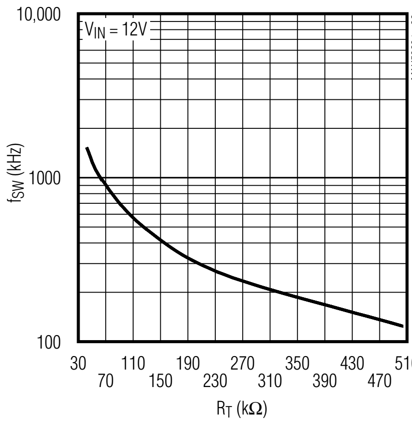


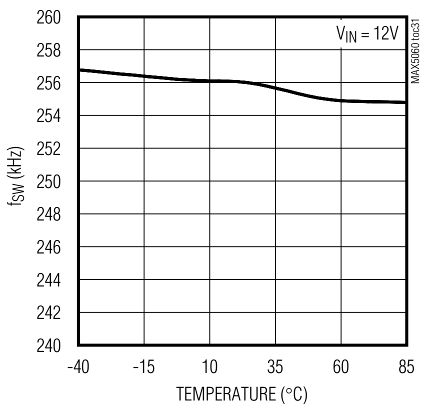
Typical Operating Characteristics (continued)

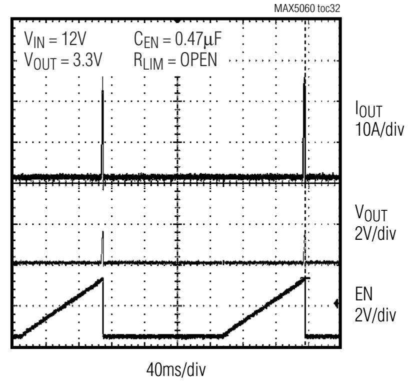
(T_A = +25°C, Figures 1 and 2, unless otherwise noted.)

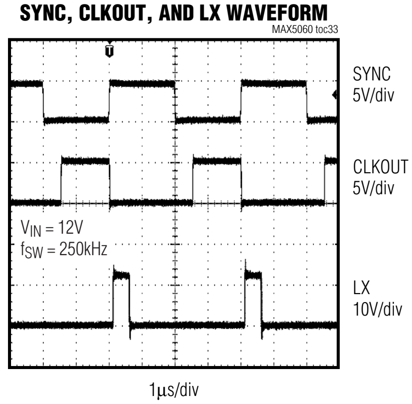












0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers

Pin Description

PIN		NAME	FUNCTION
MAX5060	MAX5061		
1	3	PGND	Power Ground. Connect PGND, low-side synchronous MOSFET's source, and V_{DD} (MAX5060)/V_{CC} (MAX5061) bypass capacitor returns together.
2, 7	8	N.C.	No Connection. Not internally connected.
3	4	DL	Low-Side Gate-Driver Output. Synchronous MOSFET gate driver.
4	5	BST	Boost Flying-Capacitor Connection. Reservoir capacitor connection for the high-side MOSFET driver supply. Connect a 0.47µF ceramic capacitor between BST and LX.
5	6	LX	Inductor Connection. Source connection for the high-side MOSFETs. Also serves as the return terminal for the high-side driver.
6	7	DH	High-Side Gate-Driver Output. Drives the gate of the high-side MOSFET.
8, 22, 25	16	SGND	Signal Ground. Ground connection for the internal control circuitry. Connect SGND and PGND together at one point near the input bypass capacitor return.
9	—	CLKOUT	Oscillator Output. Rising edge of CLKOUT is phase-shifted from rising edge of DH by 180°.
10	—	PGOOD	Power-Good Output. PGOOD is an open-drain output that goes low when the programmed output voltage falls out of regulation. The power-good comparator threshold is 90% of the programmed output voltage.
11	—	EN	Output Enable. Drive EN high or leave unconnected for normal operation. Drive EN low to shut down the power drivers. EN has an internal 15µA pullup current. Connect a capacitor from EN to SGND to program the hiccup mode duty cycle.
12	—	RT/SYNC	Switching Frequency Programming and Chip-Enable Input. Connect a resistor from RT/SYNC to SGND to set the internal oscillator frequency. Drive RT/SYNC externally to synchronize the switching frequency with system clock.
13	—	V_IOUT	Voltage-Source Output Proportional to the Output Load Current. The voltage at V_IOUT is 135 x I_{LOAD} x R_S.
14	10	LIM	Current-Limit Setting Input. Connect a resistor from LIM to SGND to set the hiccup current-limit threshold. Connect a capacitor from LIM to SGND to ignore short output overcurrent pulses.
15	—	OVI	Overvoltage Protection Circuit Input. Connect OVI to DIFF. When OVI exceeds +12.7% above the programmed output voltage, DH is latched low and DL is latched high. Toggle EN low to high or recycle the power to reset the latch.
16	11	CLP	Current-Error-Amplifier Output. Compensate the current loop by connecting an RC network to ground.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX5060	MAX5061		
17	12	EAOUT	Voltage-Error-Amplifier Output. Connect to the external gain-setting feedback resistor. The error-amplifier gain-setting resistors determine the amount of adaptive voltage positioning.
18	13	EAN	Voltage-Error-Amplifier Inverting Input. Receives a signal from the output of the differential remote-sense amplifier (MAX5060). Connect the center tap of the resistor-divider from the output to SGND (MAX5061).
19	—	DIFF	Differential Remote-Sense Amplifier Output. DIFF is the output of a precision unity-gain amplifier whose inputs are SENSE+ and SENSE-.
20	14	CSN	Current-Sense Differential Amplifier Negative Input. The differential voltage between CSN and CSP is amplified internally by the current-sense amplifier (gain = 34.5) to measure the inductor current.
21	15	CSP	Current-Sense Differential Amplifier Positive Input. The differential voltage between CSP and CSN is amplified internally by the current-sense amplifier (gain = 34.5) to measure the inductor current.
23	—	SENSE-	Differential Output-Voltage-Sensing Negative Input. SENSE- is used to sense a remote load. Connect SENSE- to V_{OUT-} or PGND at the load.
24	—	SENSE+	Differential Output-Voltage-Sensing Positive Input. SENSE+ is used to sense a remote load. Connect SENSE+ to V_{OUT+} at the load. The device regulates the difference between SENSE+ and SENSE- according to the preset reference voltage of 0.6V.
26	1	IN	Supply Voltage Connection. Connect IN to V_{CC} for a +5V system.
27	2	V_{CC}	Internal +5V Regulator Output. V_{CC} is derived from the IN voltage. Bypass V_{CC} to SGND with 4.7µF and 0.1µF ceramic capacitors. For MAX5061, connect an additional 0.1µF bypass capacitor from V_{CC} to PGND.
28	—	V_{DD}	Supply Voltage for Low-Side and High-Side Drivers. Connect a parallel combination of 0.1µF and 1µF ceramic capacitors to PGND and a 1Ω resistor to V_{CC} to filter out the high peak currents of the driver from the internal circuitry.
—	9	RT/SYNC/EN	Switching Frequency Programming and Chip-Enable Input. Connect a resistor from RT/SYNC/EN to SGND to set the internal oscillator frequency. Drive RT/SYNC/EN externally to synchronize the switching frequency with system clock. If RT/SYNC/EN is held low for 50µs, the device turns off the output drivers.
—	—	EP	Exposed Paddle. Connect the exposed paddle to a copper pad (SGND) to improve power dissipation.

Typical Application Circuit

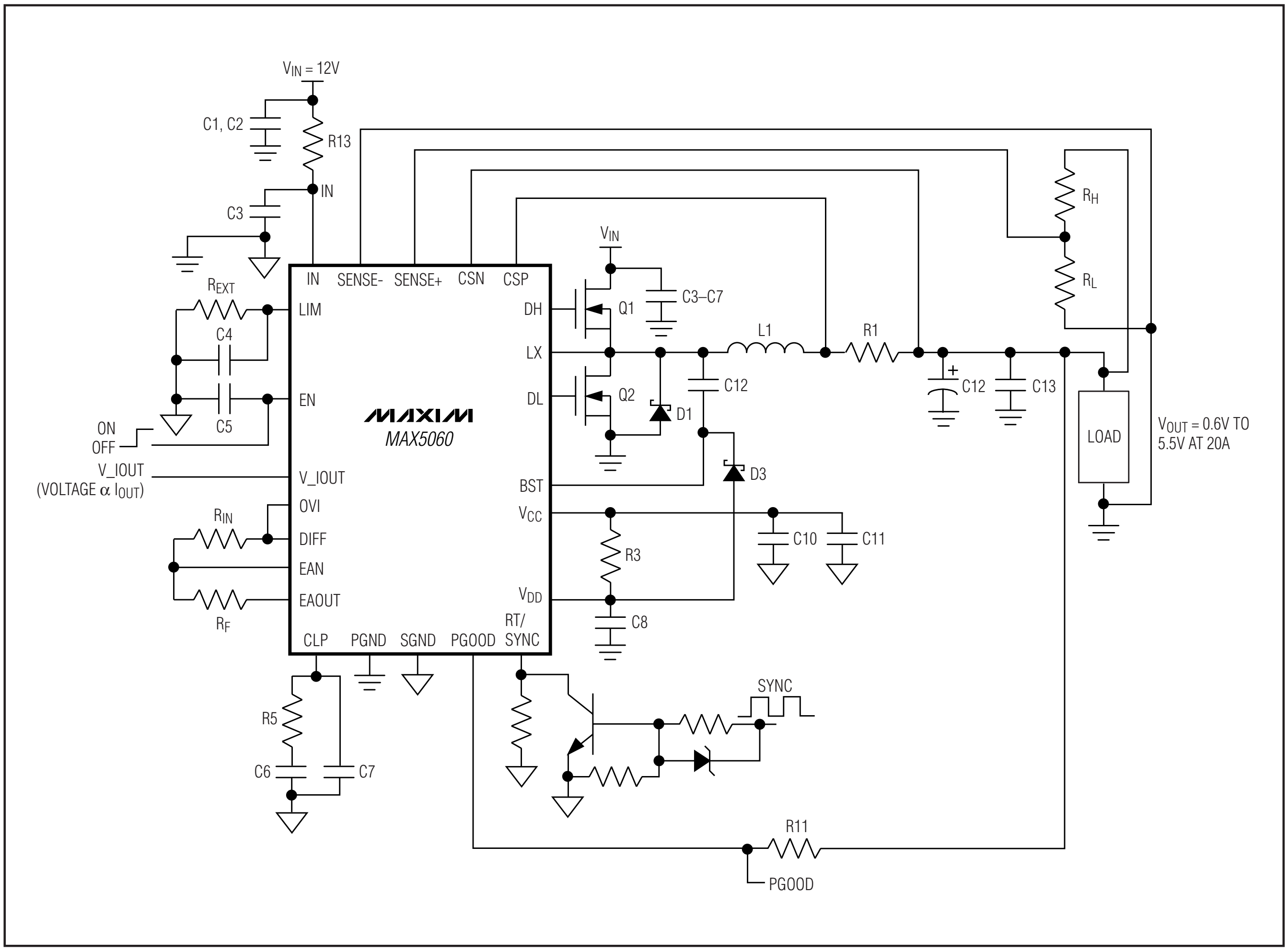


Figure 1. Typical Application Circuit, V_{IN} = 12V (MAX5060)

Typical Application Circuit (continued)

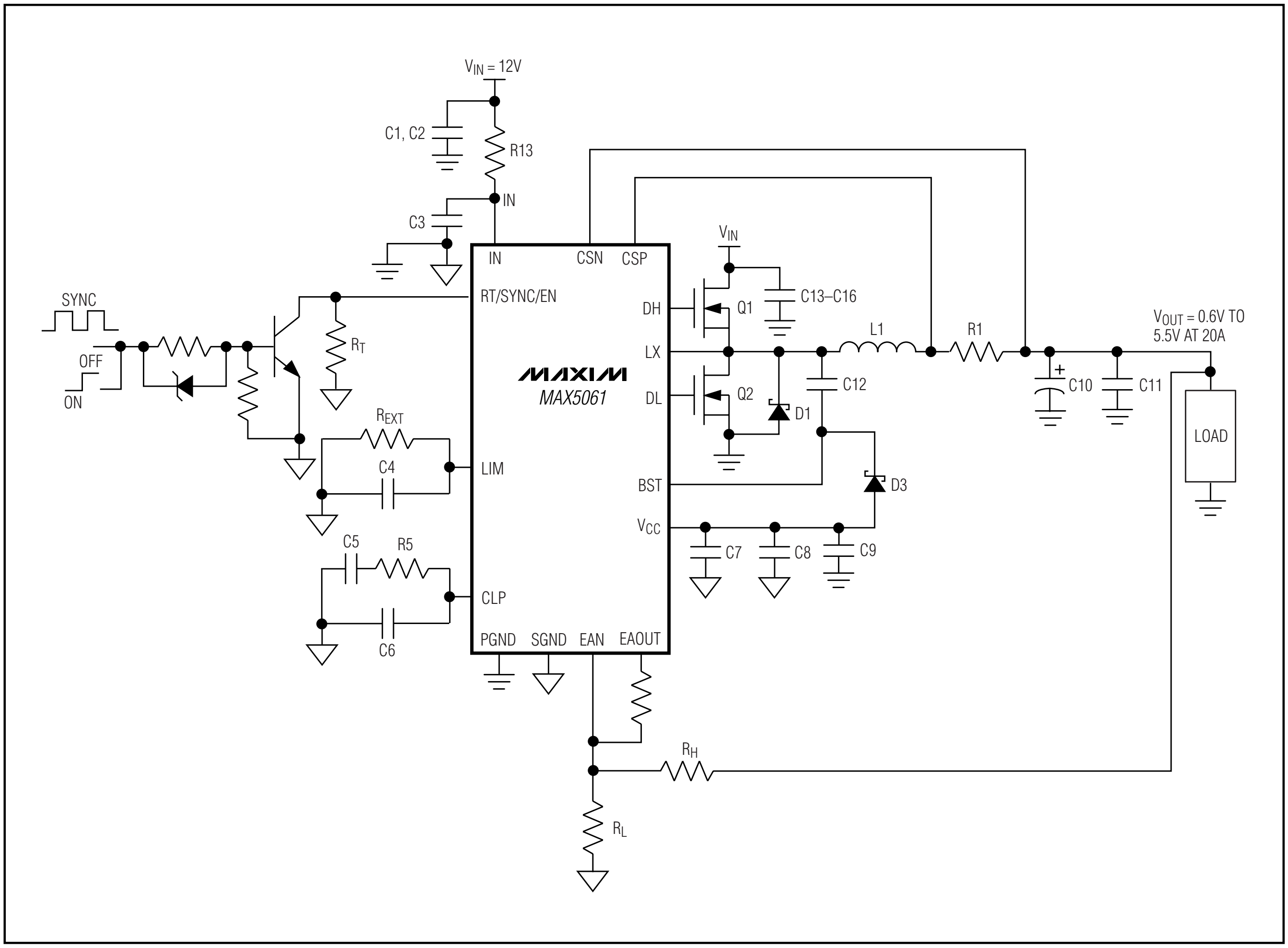


Figure 2. Typical Application Circuit, V_{IN} = +12V (MAX5061)

0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers

Block Diagram

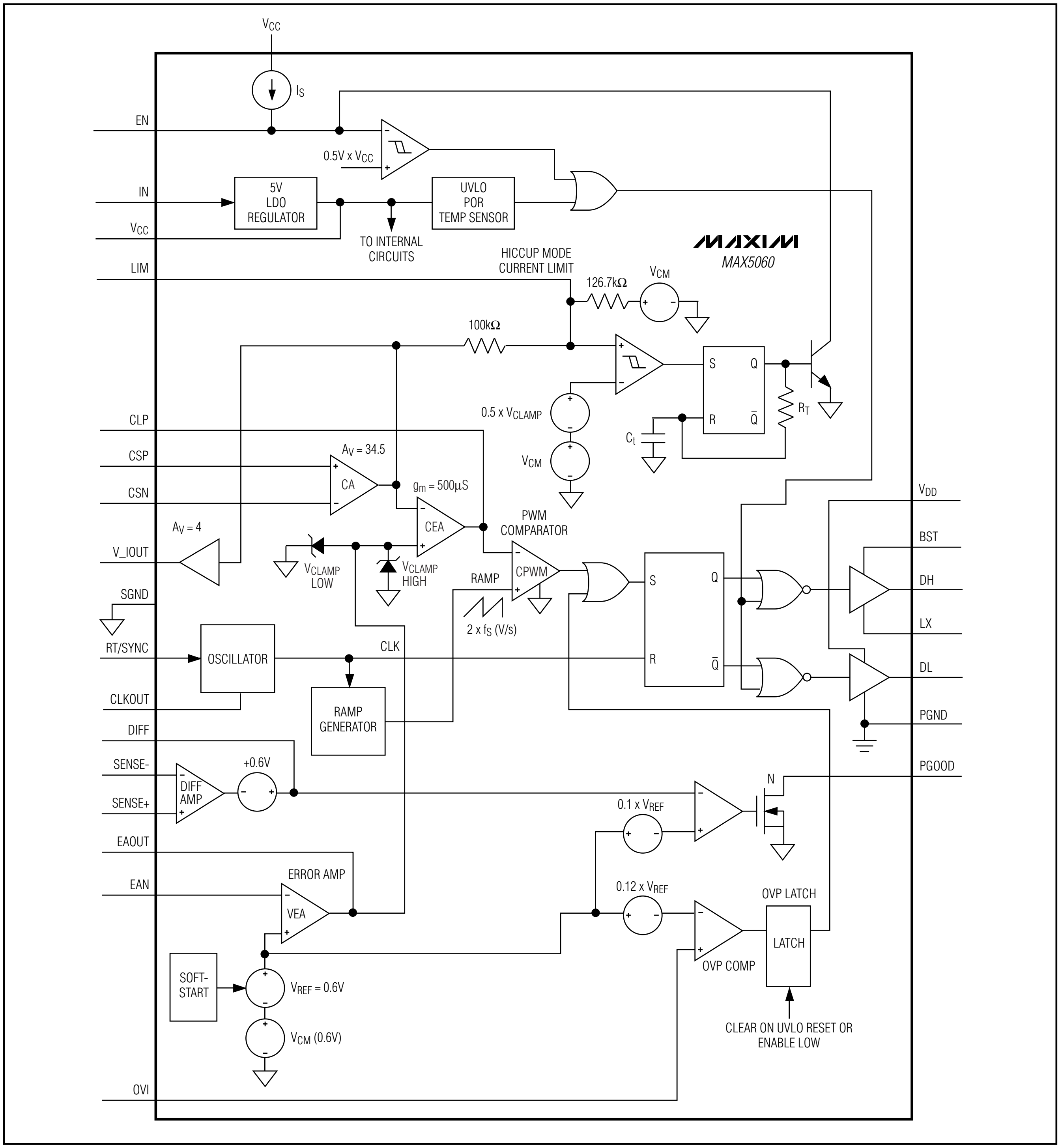


Figure 3. Functional Diagram (MAX5060)

Block Diagram (continued)

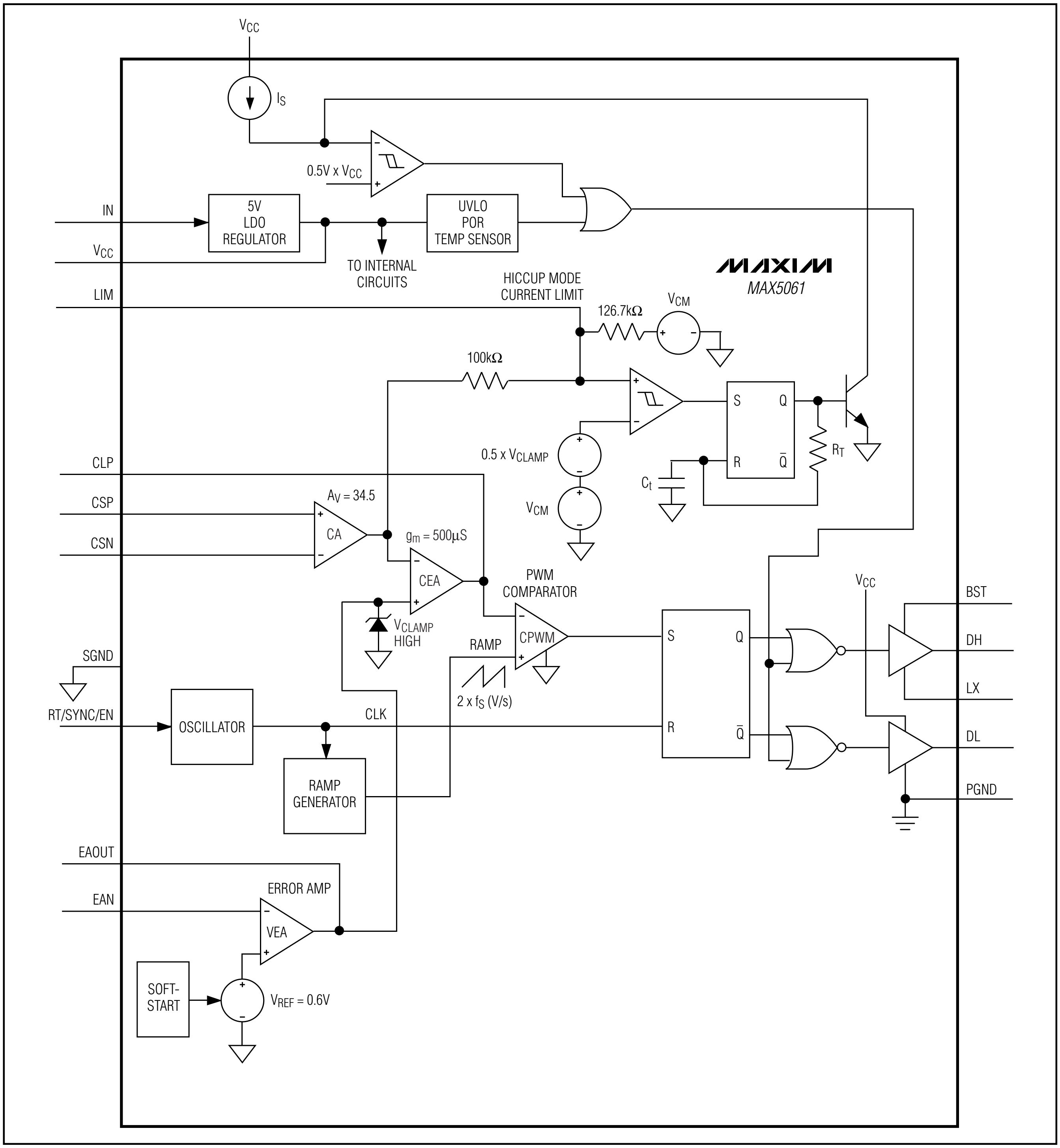


Figure 4. Functional Diagram (MAX5061)

0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers

Detailed Description

The MAX5060/MAX5061 are high-performance average-current-mode PWM controllers. The average-current-mode control technique offers inherently stable operation, reduces component derating and size by accurately controlling the inductor current. This also improves the current-sharing accuracy when paralleling multiple converters. The devices achieve high efficiency, at high current (up to 30A) with a minimum number of external components. The high- and low-side drivers source and sink up to 4A for lower switching frequencies while driving high-gate-charge MOSFETs.

The MAX5060's CLKOUT output is 180° out-of-phase with respect to the high-side driver. The CLKOUT drives a second MAX5060 or a MAX5061 regulator out-of-phase, reducing the input capacitor ripple current and increasing the load current capacity. The paralleling capability of the MAX5060/MAX5061 improves design flexibility in applications requiring upgrades (higher load).

The MAX5060/MAX5061 consist of an inner average-current-loop controlled by an outer-voltage-loop voltage-error amplifier (VEA). The combined action of the inner current loop and outer voltage loop corrects the output voltage errors by adjusting the inductor current. The inductor current is sensed across a current-sense resistor. The differential amplifier (MAX5060) senses the output right at the load for true-differential output voltage sensing. The sensed voltage is compared against internal 0.6V reference at the error-amplifier input. The output voltage can be set from 0.6V to 5.5V (IN ≥ 7V) using a resistor-divider at SENSE+ and SENSE-.

IN, V_{CC}, and V_{DD}

The MAX5060/MAX5061 accept a 4.75V to 5.5V or 7V to 28V input voltage range. All internal control circuitry operates from an internally regulated nominal voltage of 5V (V_{CC}). For input voltages of 7V or greater, the internal V_{CC} regulator steps the voltage down to 5V. The V_{CC} output voltage is a regulated 5V output capable of sourcing up to 60mA. Bypass the V_{CC} to SGND with 4.7µF and 0.1µF low-ESR ceramic capacitors for high-frequency noise rejection and stable operation. The MAX5060 uses V_{DD} to power the low-side and high-side drivers, while the MAX5061 uses the V_{CC} to power internal circuitry as well as the low- and high-side driver supply. In the case of the MAX5061, use one or more 0.1µF low-ESR ceramic capacitors between V_{CC} and PGND to reject the noise spikes due to high-current driver switching.

The TQFN-28 and TSSOP-16 are thermally enhanced packages and can dissipate up to 2.7W and 1.7W, respectively. The high-power packages allow the high-frequency, high-current buck converter to operate from a 12V or 24V bus. Calculate power dissipation in the MAX5060/MAX5061 as a product of the input voltage and the total V_{CC} regulator output current (I_{CC}). I_{CC} includes quiescent current (I_Q) and gate-drive current (I_{DD}):

$$P_D = V_{IN} \times I_{CC}$$

$$I_{CC} = I_Q + [f_{SW} \times (Q_{G1} + Q_{G2})]$$

where Q_{G1} and Q_{G2} are the total gate charge of the low-side and high-side external MOSFETs at V_{GATE} = 5V, I_Q is 3.5mA (typ), and f_{SW} is the switching frequency of the converter.

Undervoltage Lockout (UVLO)

The MAX5060/MAX5061 include an undervoltage lockout with hysteresis and a power-on-reset circuit for converter turn-on and monotonic rise of the output voltage. The UVLO rising threshold is internally set at 4.35V with a 200mV hysteresis. Hysteresis at UVLO eliminates chattering during startup.

Most of the internal circuitry, including the oscillator, turns on when the input voltage reaches 4V. The MAX5060/MAX5061 draw up to 3.5mA of current before the input voltage reaches the UVLO threshold.

Soft-Start

The MAX5060/MAX5061 has an internal digital soft-start for a monotonic, glitch-free rise of output voltage. Soft-start is achieved by the controlled rise of error amplifier dominant input in steps using a 5-bit counter and a 5-bit DAC. The soft-start DAC generates a linear ramp from 0 to 0.7V. This voltage is applied to the error amplifier at a third (noninverting) input. As long as the soft-start voltage is lower than the reference voltage, the system will converge to that lower reference value. Once the soft-start DAC output reaches 0.6V, the reference takes over and the DAC output continues to climb to 0.7V assuring that it is out of the way of the reference voltage.

Internal Oscillator

The internal oscillator generates a clock with the frequency proportional to the inverse of R_T. The oscillator frequency is adjustable from 125kHz to 1.5MHz with better than 8% accuracy using a single resistor connected from RT/SYNC to SGND (MAX5060) and from RT/SYNC/EN to SGND (MAX5061). The frequency accuracy avoids the over-design, size, and cost of passive filter components like inductors and capacitors. Use the following equation to calculate the oscillator frequency:

for $120k\Omega \le R_T \le 500k\Omega$:

$$R_T = \frac{6.25 \times 10^{10}}{f_{SW}}$$

for $40k\Omega \le R_T \le 120k\Omega$:

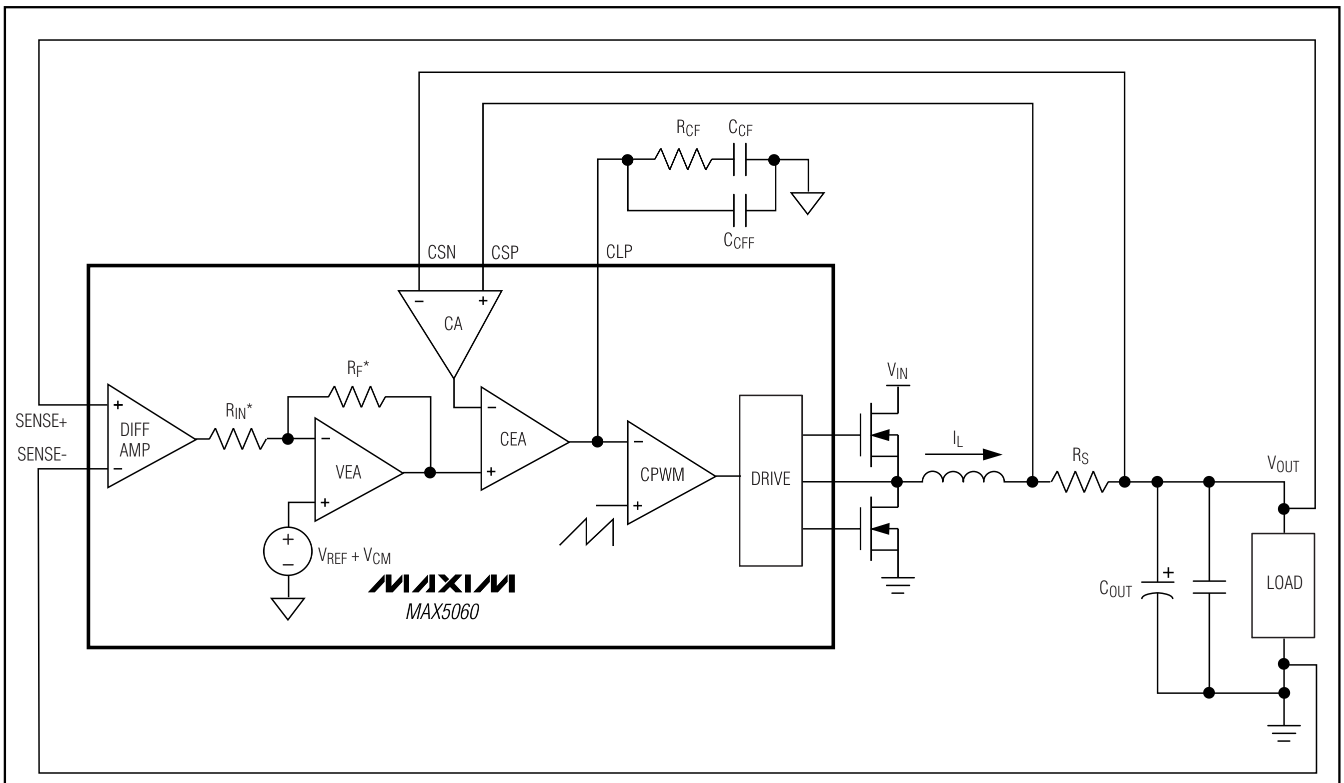
$$R_T = \frac{6.40 \times 10^{10}}{f_{SW}}$$

The oscillator also generates a $2V_{P-P}$ voltage-ramp signal for the PWM comparator and a 180° out-of-phase clock signal for CLKOUT (MAX5060) to drive a second DC-DC converter out-of-phase.

Synchronization

The MAX5060/MAX5061 can be easily synchronized by connecting an external clock to RT/SYNC (MAX5060) or RT/SYNC/EN (MAX5061). If an external clock is present, then the internal oscillator is disabled and the external clock is used to run the MAX5060/MAX5061. If the external clock is removed, the absence of clock for 32µs is detected and the circuit starts switching from the internal oscillator. Pulling RT/SYNC on the MAX5060 or RT/SYNC/EN on the MAX5061 to ground for at least 50µs disables the converter.

Use an open-collector transistor to synchronize the MAX5060/MAX5061 with the external system clock (see Figures 1 and 2).



*RF AND RIN ARE EXTERNAL.

Figure 5. MAX5060 Control Loop

0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers

Control Loop

The MAX5060/MAX5061 use an average-current-mode control scheme to regulate the output voltage (Figure 5). The main control loop consists of an inner current loop and an outer voltage loop. The inner loop controls the output current (I_{PHASE}), while the outer loop controls the output voltage. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a single-pole system.

The current loop consists of a current-sense resistor (R_{SENSE}), a current-sense amplifier (CA), a current-error amplifier (CEA), an oscillator providing the carrier ramp, and a PWM comparator (CPWM) (Figure 6). The precision CA amplifies the sense voltage across RS by a factor of 34.5. The inverting input to the CEA senses the CA output. The CEA output is the difference between the voltage-error-amplifier output (EAOUT) and the amplified voltage from the CA. The RC compensation networks connected to CLP provide external frequency compensation for the CEA. The start of every clock cycle enables the high-side drivers and initiates a PWM ON cycle. Comparator CPWM compares the output voltage from the CEA with a 0 to 2V ramp from the oscillator. The PWM ON cycle terminates when the ramp voltage exceeds the error voltage.

The MAX5060 outer voltage control loop consists of the differential amplifier (DIFF AMP), reference voltage, and VEA. The unity-gain differential amplifier provides true-differential remote sensing of the output voltage. The differential amplifier output connects to the inverting input (EAN) of the VEA. For MAX5061, the DIFF AMP is bypassed and the inverting input is available to the pin for direct feedback. The noninverting input of the VEA is internally connected to an internal precision reference voltage. The MAX5060/MAX5061 reference voltage is set to 0.6V. The VEA controls the inner current loop (*Figure* 4). Use a resistive feedback network to set the VEA gain as required by the adaptive voltage-positioning circuit (see the *Adaptive Voltage Positioning* section).

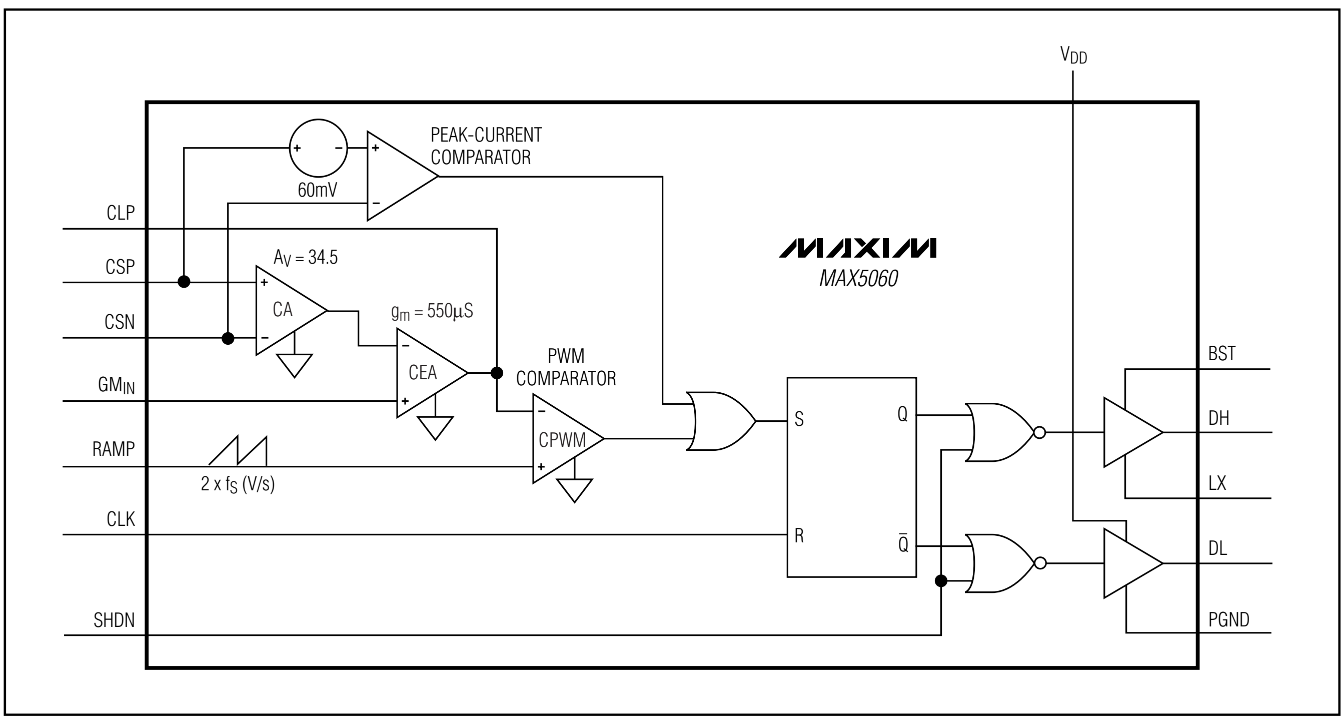


Figure 6. Phase Circuit

Current-Sense Amplifier

The differential current-sense amplifier (CA) provides a DC gain of 34.5. The maximum input offset voltage of the current-sense amplifier is 1mV and the common-mode voltage range is 0 to 5.5V (IN = 7V to 28V). The current-sense amplifier senses the voltage across a current-sense resistor. The maximum common-mode voltage is 3.6V when V_{IN} = 5V. The common-mode voltage range determines the maximum output voltage of the buck converter.

Peak-Current Comparator

The peak-current comparator provides a path for fast cycle-by-cycle current limit during extreme fault conditions such as an output inductor malfunction (Figure 5). Note the average current-limit threshold of 26.9mV still limits the output current during short-circuit conditions. To prevent inductor saturation, select an output inductor with a saturation current specification greater than the average current limit. Proper inductor selection ensures that only the extreme conditions trip peak-current comparator, such as a broken output inductor. The 60mV threshold for triggering the peak-current limit is twice the full-scale average current-limit voltage threshold. The peak-current comparator has only a 260ns delay.

Current-Error Amplifier

The MAX5060/MAX5061 has a transconductance current-error amplifier (CEA) with a typical g_m of 550µS and 320µA output sink- and source-current capability. The current-error amplifier output CLP, serves as the inverting input to the PWM comparator. CLP is externally accessible to provide frequency compensation for the inner current loops (Figure 5). Compensate (CEA) so the inductor current down slope, which becomes the up slope to the inverting input of the PWM comparator, is less than the slope of the internally generated voltage ramp (see the *Compensation* section).

PWM Comparator and R-S Flip-Flop

The PWM comparator (CPWM) sets the duty cycle for each cycle by comparing the output of the current-error amplifier to a $2V_{P-P}$ ramp. At the start of each clock cycle, an R-S flip-flop resets and the high-side driver (DH) turns on. The comparator sets the flip-flop as soon as the ramp voltage exceeds the CLP voltage, thus terminating the ON cycle (Figure 5).

Differential Amplifier (MAX5060)

The differential amplifier (DIFF AMP) facilitates output-voltage remote sensing at the load (Figure 5). It provides true-differential output voltage sensing while rejecting the common-mode voltage errors due to high-current ground paths. Sensing the output voltage directly at the load provides accurate load voltage sensing in high-current environments. The VEA provides the difference between the differential amplifier output (DIFF) and the desired output voltage. The differential amplifier has a bandwidth of 3MHz. The difference between SENSE+ and SENSE- is regulated to 0.6V for the MAX5060. Connect SENSE+ to the center of the resistive divider from the output to SENSE-. Connect SENSE- to PGND near the load.

Voltage-Error Amplifier

The VEA sets the gain of the voltage control loop. The VEA determines the error between the differential amplifier output and the internal reference voltage.

The VEA output clamps to 930mV relative to the internally generated common-mode voltage (V_{CM}, 0.6V), thus limiting the maximum output current. The maximum average current-limit threshold is equal to the maximum clamp voltage of the VEA divided by the gain (34.5) of the current-sense amplifier. This results in accurate settings for the average maximum current for each phase. Set the VEA gain using R_F and R_{IN} (see Figures 1 and 2) for the amount of output voltage positioning required within the rated current range as discussed in the *Adaptive Voltage Positioning* section. The finite gain of the VEA introduces an error in the output voltage setting. Use the following equation to calculate the output voltage at no load condition.

$$V_{OUT(NL)} = \left(1+\frac{R_{IN}}{R_F}\right)\times\left(\frac{R_H+R_L}{R_L}\right)\times V_{REF}$$

where R_H and R_L are the feedback resistor network (see the *Typical Application Circuits*) and V_{REF} = 0.6V.

Adaptive Voltage Positioning

Powering new-generation processors requires new techniques to reduce cost, size, and power dissipation. Voltage positioning reduces the total number of output capacitors to meet a given transient response requirement. Setting the no-load output voltage slightly higher than the output voltage during nominally loaded conditions allows a larger downward-voltage excursion when the output current suddenly increases. Regulating at a lower output voltage under a heavy load allows a larger upward-voltage excursion when the output current suddenly decreases. Allowing a larger voltage-step excursion reduces the required number of output capacitors or allows for the use of higher ESR capacitors.

Voltage positioning may require the output to regulate away from a center value. Define the center value as the voltage where the output drops ($\Delta V_{OUT}/2$) at one half the maximum output current (Figure 7).

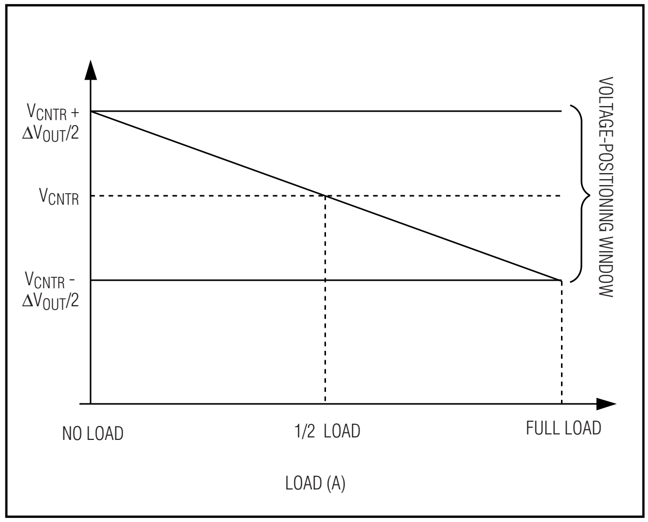


Figure 7. Defining the Voltage-Positioning Window

Set the voltage-positioning window (ΔV_{OUT}) using the resistive feedback of the voltage-error amplifier (VEA). Use the following equations to calculate the voltage-positioning window (Figure 5):

$$\Delta V_{OUT} = \frac{I_{OUT} \times R_{IN}}{G_C \times R_F} \times \frac{R_H + R_L}{R_L}$$

$$G_C = \frac{0.0289}{R_S}$$

R_{IN} and R_F are the input and feedback resistors of VEA. G_C is the current-loop transconductance and R_S is the current-sense resistor.

MOSFET Gate Drivers (DH_, DL_)

The high-side (DH) and low-side (DL) drivers drive the gates of external n-channel MOSFETs (Figures 1 and 2). The drivers' 4A peak sink- and source-current capability provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced cross-conduction losses. For modern CPU voltage-regulating module applications, where the duty cycle is less than 50%, choose high-side MOSFETs (Q1) with a moderate $R_{DS(ON)}$ and a very low gate charge. Choose low-side MOSFETs (Q2) with very low $R_{DS(ON)}$ and moderate gate charge. Size the high-side and low-side MOSFETs to handle the peak and RMS currents during overload conditions.

The driver block also includes a logic circuit that provides an adaptive nonoverlap time to prevent shoot-through currents during transition. The typical nonoverlap time is 35ns between the high-side and low-side MOSFETs.

BST

The MAX5060 uses V_{DD} to power the low- and high-side MOSFET drivers. The low- and high-side drivers in the MAX5061 are powered from V_{CC}. The high-side driver derives its power through a bootstrap capacitor and V_{DD} supplies power internally to the low-side driver. Connect a 0.47µF low-ESR ceramic capacitor between BST and LX. Connect a Schottky rectifier from BST to V_{DD} on the MAX5060, or to V_{CC} on the MAX5061. Reduce the PC board area formed by the boost capacitor and rectifier.

Protection

The MAX5060 includes a power-good generator (PGOOD) for undervoltage protection (UVP), and a reverse current-limit protection; the MAX5060/MAX5061 include a hiccup current-limit protection to prevent damage to the powered electronic circuits. Additionally, the MAX5060 includes output overvoltage protection (OVP).

PGOOD Generator (MAX5060)

A PGOOD comparator compares the differential amplifier output (DIFF) against 0.90 times the set output voltage for undervoltage monitoring (see Figure 8). Use a 10kΩ pullup resistor from PGOOD to a voltage source less than or equal to V_{CC}.

Current Limit

The VEA output is clamped to 930mV with respect to the common-mode voltage (V_{CM}). Average current-mode control has the ability to limit the average current sourced by the converter during a fault condition. When a fault condition occurs, the VEA output clamps to 930mV with respect to the common-mode voltage (0.6V) to limit the maximum current sourced by the converter to I_{LIMIT} = 26.9mV/R_S.

The hiccup current limit overrides the average current limit. The MAX5060/MAX5061 include hiccup current-limit protection to reduce the power dissipation during a fault condition. The hiccup current-limit circuit derives inductor current information from the output of the current amplifier. This signal is compared against one half of $V_{CLAMP(EA)}$. With no resistor connected from the LIM pin to ground, the hiccup current limit is set at 90% of the full-load average current limit. Use R_{EXT} to increase the hiccup current limit from 90% to 100% of the full-load average limit (see Figures 1 and 2). The hiccup current limit can be disabled by connecting LIM to SGND. In this case, the circuit will follow the average current-limit action during overload conditions.

An internal clamp limits the continuous reverse current the buck converter sinks when a higher voltage is applied at the output. The reverse current limit translated at the current-amplifier input is -2.3mV (typ). The maximum reverse current the converter sinks depends on the current-sense resistor. Normally it is about 10% of the full load current.

Overvoltage Protection (OVP) (MAX5060)

The OVP comparator compares the OVI input to the overvoltage threshold. The overvoltage threshold is typically +12.7% above the internal 0.6V reference voltage. A detected overvoltage event latches the comparator output forcing the power stage into the OVP state. In the OVP state, the high-side MOSFET turns off and the low-side MOSFET latches on. Connect DIFF to OVI for differential output sensing and overvoltage protection. Alternately, use a separate sensing network from V_{OUT} to SGND. Connect OVI to the center tap of a resistor-divider from V_{OUT} to SGND. In this case, the center tap is compared against 1.276V. Add an RC delay to reduce the sensitivity of the overvoltage circuit and avoid nuisance tripping of the converter (Figure 9). Disable the overvoltage function by connecting OVI to SGND.

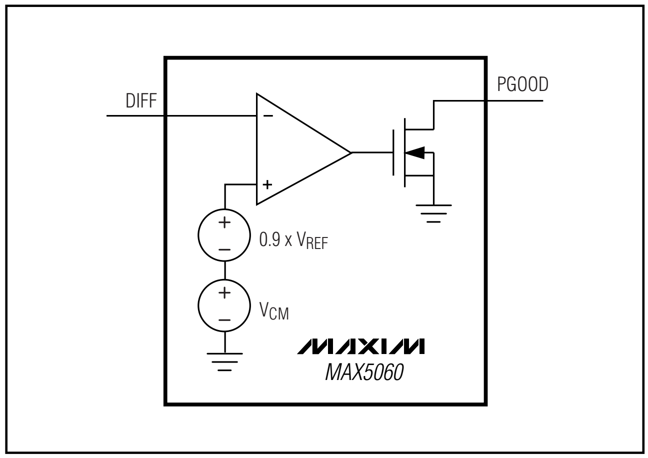


Figure 8. PGOOD Generator

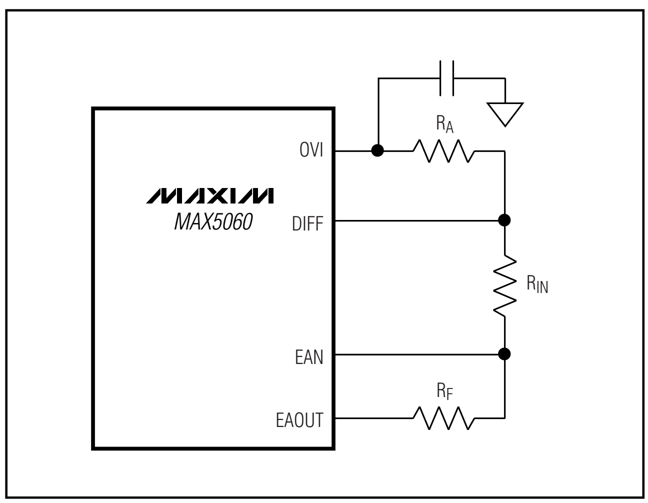


Figure 9. Overvoltage Protection Input Delay

Parallel Operation

For applications requiring large output current, parallel two or more MAX5060s (multiphase operation) to increase the available output current. The paralleled converters operate at the same switching frequency but different phases keep the input capacitor ripple RMS currents to a minimum. The MAX5060 provides the clock output (CLKOUT), which is 180° out-of-phase with respect to DH. For the MAX5061, the out-of-phase clock can be easily generated using a simple inverter and driving it from the LX node. Use CLKOUT to drive the second DC-DC converter to double the effective switching frequency and reduce the input capacitor ripple current (see Figure 10).

To drive multiple converters out-of-phase, use a delay circuit to set 90° of phase shift (4 paralleled converters), or 60° of phase shift (6 converters in parallel). Designate one converter as master and the remaining converters as slaves. Connect the master and slave controllers in a daisy-chain configuration as shown in Figure 11. Choose the appropriate phase shift for minimum ripple currents at the input and output capacitors. The master controller senses the output differential voltage through SENSE+ and SENSE- and generates the DIFF voltage. Disable the voltage sensing of the slaved controllers by leaving DIFF unconnected (floating). Figure 11 shows a typical application circuit using four MAX5060s. This circuit provides two phases at a 12V input voltage and a 0.6V to 5V output voltage range.

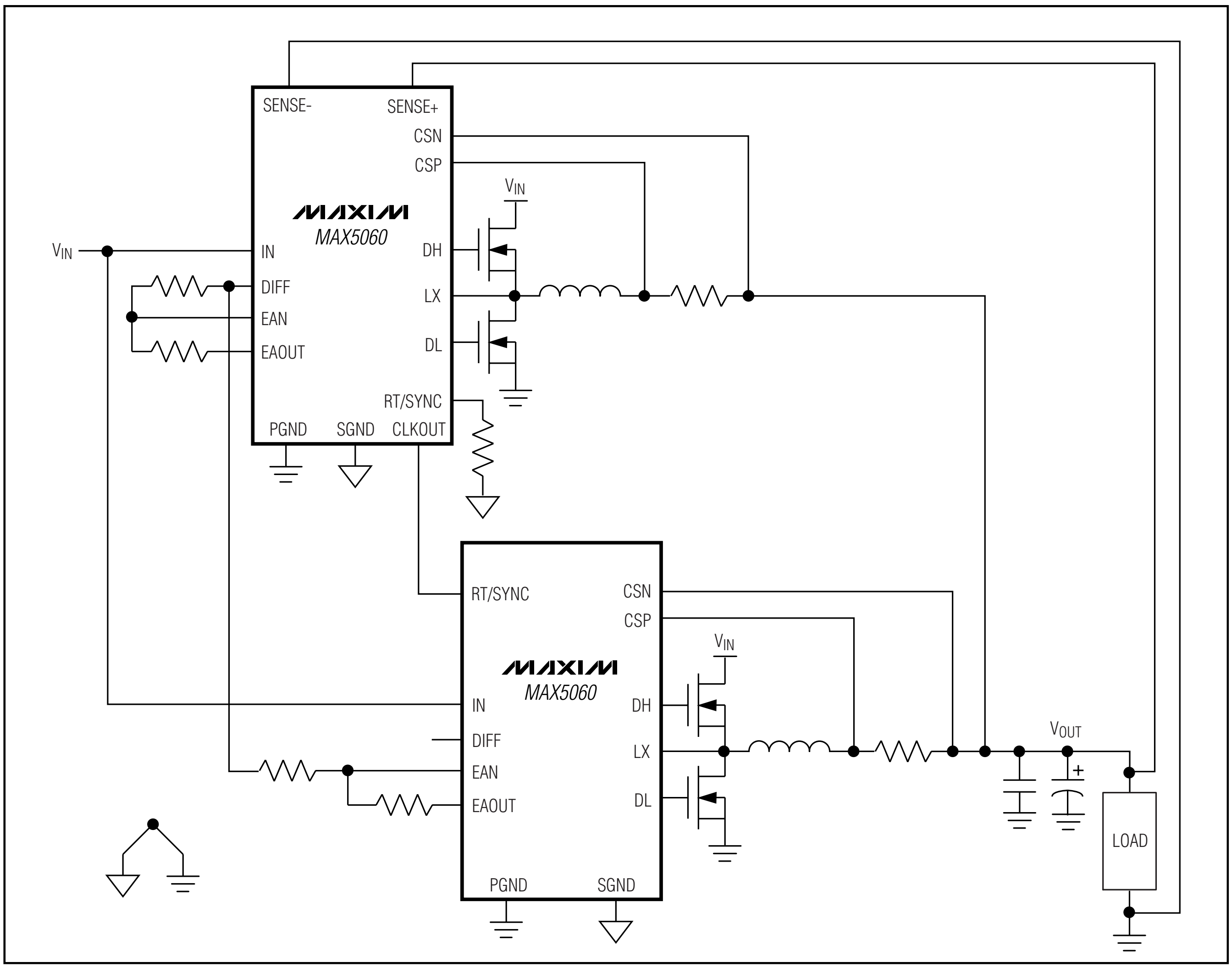


Figure 10. Parallel Configuration of MAX5060

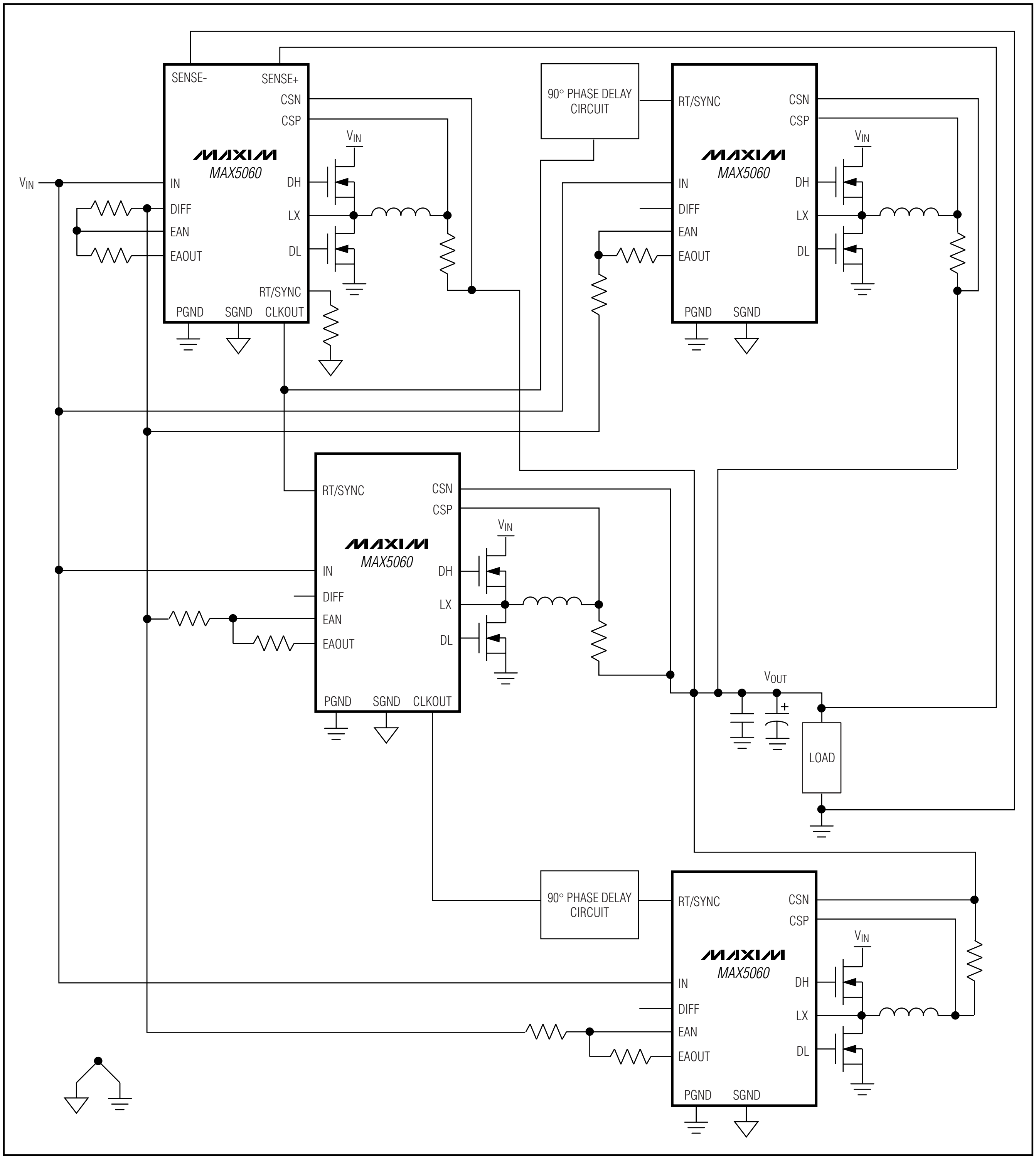


Figure 11. Parallel Configuration of Multiple MAX5060s

0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers

Applications Information

Inductor Selection

The switching frequency, peak inductor current, and allowable ripple at the output determine the value and size of the inductor. Selecting higher switching frequencies reduces the inductance requirement, but at the cost of lower efficiency. The charge/discharge cycle of the gate and drain capacitances in the switching MOSFETs create switching losses. The situation worsens at higher input voltages, since switching losses are proportional to the square of the input voltage. The MAX5060 can operate up to 1.5MHz, however for V_{IN} > +12V, use lower switching frequencies to limit the switching losses.

Use the following equation to determine the minimum inductance value:

$$L_{MIN} = \frac{(V_{INMAX} - V_{OUT}) \times V_{OUT}}{V_{INMAX} \times f_{SW} \times \Delta I_L}$$

Choose ΔI_L equal to approximately 40% of the output current. Since ΔI_L affects the output-ripple voltage, the inductance value may need minor adjustment after choosing the output capacitors. Higher values reduce the output ripple, but at the cost of degraded transient response. Lower values have higher output ripple but better transient response. Also, lower inductor values correspond to smaller magnetics.

Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. Particular applications may require custom-made inductors. Use high-frequency core material for custom inductors. High ΔI_L causes large peak-to-peak flux excursion, which increases the core losses at higher frequencies. The high-frequency operation coupled with high ΔI_L reduces the required minimum inductance and even makes the use of planar inductors possible. The advantages of using planar magnetics include low-profile design, excellent current-sharing between modules due to the tight control of parasitics, and low cost.

For example, calculate the minimum inductance at $V_{IN(MAX)}$ = 13.2V, V_{OUT} = 1.8V, ΔI_L = 8A, and f_{SW} = 330kHz:

$$L_{MIN} = \frac{(13.2 - 1.8) \times 1.8}{13.2 \times 330k \times 8} = 0.6\mu H$$

The average-current-mode control feature of the MAX5060/MAX5061 limits the maximum peak inductor current and prevents the inductor from saturating. Choose an inductor with a saturating current greater than the worst-case peak inductor current. The hiccup current-limit circuit is masked during startup to avoid unintentional hiccup when large output capacitors are used.

Use the following equation to determine the worst-case inductor current:

$$L_{LPEAK} = \frac{V_{CL}}{R_S} + \frac{\Delta I_L}{2}$$

where R_S is the sense resistor and V_{CL} = 0.0282V.

Switching MOSFETs

When choosing a MOSFET for voltage regulators, consider the total gate charge, $R_{DS(ON)}$, power dissipation, and package thermal impedance. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs optimized for high-frequency switching applications.

The average current from the MAX5060/MAX5061 gate-drive output is proportional to the total capacitance it drives at DH and DL. The power dissipated in the MAX5060/MAX5061 is proportional to the input voltage and the average drive current. See the *IN, V_{CC}, and V_{DD}* section to determine the maximum total gate charge allowed from the combined driver outputs.

The gate charge and drain capacitance (CV^2) loss, the cross-conduction loss in the upper MOSFET due to finite rise/fall time, and the I^2R loss due to RMS current in the MOSFET $R_{DS(ON)}$ account for the total losses in the MOSFET. Estimate the power loss ($PD_{MOS\_}$) caused by the high-side and low-side MOSFETs using the following equations:

$$PD_{MOS-HI} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}}{4}\right) + \left(1.4R_{DS(ON)} \times I^2_{RMS-HI}\right)$$

where Q_G, $R_{DS(ON)}$, t_R, and t_F are the upper-switching MOSFET's total gate charge, on-resistance at +25°C, rise time, and fall time, respectively.

$$I_{RMS-HI} = \sqrt{\left(I^2DC + I^2PK + I_{DC} \times I_{PK}\right) \times \frac{D}{3}}$$

where D = V_{OUT}/V_{IN}, I_{DC} = (I_{OUT} - $\Delta I_L/2$) and I_{PK} = (I_{OUT} + $\Delta I_L/2$).

$$PD_{MOS-LO} = \left(Q_G \times V_{DD} \times f_{SW}\right) + \left(\frac{2 \times C_{OSS} \times V_{IN}^2 \times f_{SW}}{3}\right) + \left(1.4R_{DS(ON)} \times I^2{}_{RMS-LO}\right)$$

$$I_{RMS-LO} = \sqrt{\left(I^2DC + I^2PK + I_{DC} \times I_{PK}\right) \times \frac{(1-D)}{3}}$$

where C_{OSS} is the MOSFET drain-to-source capacitance.

For example, from the typical specifications in the *Applications Information* section with V_{OUT} = 1.8V, the high-side and low-side MOSFET RMS currents are 7.8A and 18.5A, respectively for 20A. Ensure that the thermal impedance of the MOSFET package keeps the junction temperature at least +25°C below the absolute maximum rating. Use the following equation to calculate maximum junction temperature:

$$T_J = (PD_{MOS} \times \theta_{JA}) + T_A$$

where θ_{JA} and T_A are the junction-to-ambient thermal impedance and ambient temperature, respectively.

Input Capacitors

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. Increasing switching frequency or paralleling multiple out-of-phase converters lowers the peak-to-average current ratio, yielding a lower input capacitance requirement for the same load current.

The input ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high-ripple-current capability at the input. Assume the contributions from the ESR and capacitor discharge are equal to 30% and 70%, respectively. Calculate the input capacitance and ESR required for a specified ripple using the following equation:

$$ESR_{IN} = \frac{(\Delta V_{ESR})}{\left(I_{OUT} + \frac{\Delta I_L}{2}\right)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where I_{OUT} is the output current of the converter.

For example, at V_{OUT} = 1.8V, the ESR and input capacitance are calculated for the input peak-to-peak ripple of 100mV or less yielding an ESR and capacitance value of 1.25mΩ and 110µF.

Output Capacitors

The worst-case peak-to-peak and capacitor RMS ripple current, the allowable peak-to-peak output ripple voltage, and the maximum deviation of the output voltage during step loads determine the capacitance and the ESR requirements for the output capacitors.

In buck converter design, the output-current waveform is continuous and this reduces peak-to-peak ripple current in the output capacitor equal to the inductor ripple current. Calculate the capacitance, the ESR of the output capacitor, and the RMS ripple current rating of the output capacitor based on the following equations.

$$ESR_{OUT} = \frac{\Delta V_{OESR}}{\Delta I_L}$$

$$C_{OUT} = \frac{\Delta I_L}{8 \times \Delta V_{OQ} \times f_{SW}}$$

where ΔV_{OESR} and ΔV_{OQ} are the output-ripple contributions due to ESR and the discharge of output capacitor, respectively.

In the dynamic load environment, the allowable deviation of output voltage during the fast transient load dictates the output capacitance and ESR. The output capacitors supply the load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The resistive drop across the capacitor ESR and capacitor discharge causes a voltage drop during a step load. Use a combination of SP polymer and ceramic capacitors for better transient load and ripple/noise performance.

Keep the maximum output voltage deviation less than or equal to the adaptive voltage-positioning window (ΔV_{OUT}). Assume 50% contribution each from the output capacitance discharge and the ESR drop. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

where I_{STEP} is the load step and $t_{RESPONSE}$ is the response time of the controller. Controller response time depends on the control-loop bandwidth.

Current Limit

In addition to the average current limit, the MAX5060/MAX5061 also have hiccup current limit. The hiccup current limit is set to 10% below the average current limit to ensure that the circuit goes in hiccup mode during continuous output short circuit. Connecting a resistor from LIM to ground increases the hiccup current limit, while shorting LIM to ground disables the hiccup current-limit circuit.

Average Current Limit

The average-current-mode control technique of the MAX5060/MAX5061 accurately limits the maximum output current. The MAX5060/MAX5061 sense the voltage across the sense resistor and limit the peak inductor current (I_{L-PK}) accordingly. The ON cycle terminates when the current-sense voltage reaches 25.5mV (min). Use the following equation to calculate the maximum current-sense resistor value:

$$R_S = \frac{0.0255}{I_{OUT}}$$

$$PD_R = \frac{0.75 \times 10^{-3}}{R_S}$$

where PD_R is the power dissipation in the sense resistors. Select a 5% lower value of R_S to compensate for any parasitics associated with the PC board. Also, select a non-inductive resistor with the appropriate power rating.

Hiccup Current Limit

The hiccup current-limit value is always 10% lower than the average current-limit threshold, when LIM is left unconnected. Connect a resistor from LIM to SGND to increase the hiccup current-limit value from 90% to 100% of the average current-limit value. The average current-limit architecture accurately limits the average output current to its current-limit threshold. If the hiccup current limit is programmed to be equal or above the average current-limit value, the output current will not reach the point where the hiccup current limit can trigger. Program the hiccup current limit at least 5% below the average current limit to ensure that the hiccup current-limit circuit triggers during overload. See the Hiccup Current Limit vs. R_{EXT} graph in the *Typical Operating Characteristics*.

Reverse Current Limit (MAX5060)

The MAX5060 limits the reverse current in case V_{BUS} is higher than the preset output voltage. Calculate the maximum reverse current based on V_{CLR}, the reverse-current-limit threshold and the current-sense resistor.

$$I_{REVERSE} = \frac{V_{CLR}}{R_S}$$

where $I_{REVERSE}$ is the total reverse current sink into the converter and V_{CLR} = 2.3mV (typ).

Compensation

The main control loop consists of an inner current loop and an outer voltage loop. The MAX5060/MAX5061 use an average current-mode control scheme to regulate the output voltage (Figure 5). I_{PHASE} is the inner average current loop. The VEA output provides the controlling voltage for this current source. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a single-pole system.

A resistive feedback network around the VEA provides the best possible response, since there are no capacitors to charge and discharge during large-signal excursions. R_F and R_{IN} determine the VEA gain. Use the following equation to calculate the value of R_F:

$$R_F = \frac{I_{OUT} \times R_{IN}}{G_C \times \Delta V_{OUT}}$$

$$G_C = \frac{0.0289}{R_S}$$

where G_C is the current-loop transconductance and R_S is the value of the sense resistor.

When designing the current-control loop ensure that the inductor downslope (when it becomes an upslope at the CEA output) does not exceed the ramp slope. This is a necessary condition to avoid sub-harmonic oscillations similar to those in peak current-mode control with insufficient slope compensation.

Use the following equation to calculate the resistor R_{CF}:

$$R_{CF} \leq \frac{2 \times f_{SW} \times L \times 10^2}{V_{OUT} \times R_S}$$

C_{CF} provides a low-frequency pole while R_{CF} provides a midband zero. Place a zero (f_Z) to obtain a phase bump at the crossover frequency. Place a high-frequency pole (f_P) at least a decade away from the crossover frequency to reduce the influence of the switching noise and achieve maximum phase margin.

Use the following equations to calculate C_{CF} and C_{CFF}:

$$C_{CF} = \frac{1}{2 \times \pi \times f_Z \times R_{CF}}$$

$$C_{CFF} = \frac{1}{2 \times \pi \times f_P \times R_{CF}}$$

Power Dissipation

The TQFN-28 and TSSOP-16 are thermally enhanced packages and can dissipate about 2.7W and 1.7W, respectively. The high-power packages make the high-frequency, high-current buck converter possible to operate from a 12V or 24V bus. Calculate power dissipation in the MAX5060/MAX5061 as a product of the input voltage and the total V_{CC} regulator output current (I_{CC}). I_{CC} includes quiescent current (I_Q) and gate-drive current (I_{DD}):

$$P_D = V_{IN} \times I_{CC}$$

$$I_{CC} = I_Q + [f_{SW} \times (Q_{G1} + Q_{G2})]$$

where Q_{G1} and Q_{G2} are the total gate charge of the low-side and high-side external MOSFETs at V_{GATE} = 5V, I_Q is estimated from the Supply Current (I_Q) vs. Frequency graph in the *Typical Operating Characteristics*, and f_{SW} is the switching frequency of the converter.

Use the following equation to calculate the maximum power dissipation (P_{DMAX}) in the chip at a given ambient temperature (T_A) :

MAX5060:

$$P_{DMAX} = 34.5 \times (150 - T_A) \text{..............mW}$$

MAX5061:

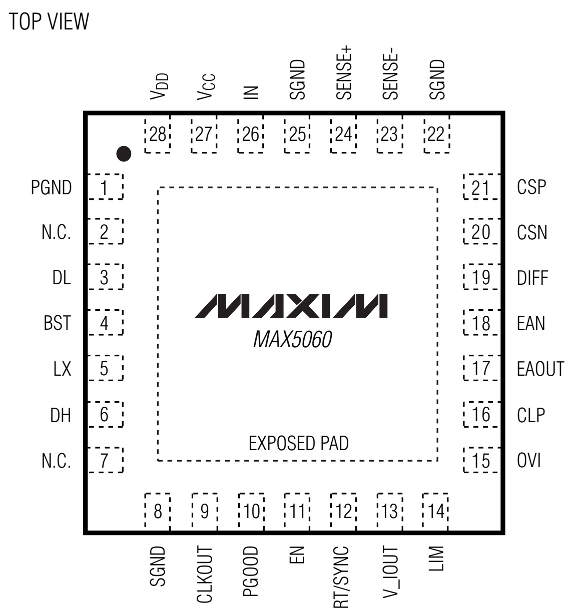
$$P_{DMAX} = 21.3 \times (150 - T_A) \text{..............mW}$$

PC Board Layout

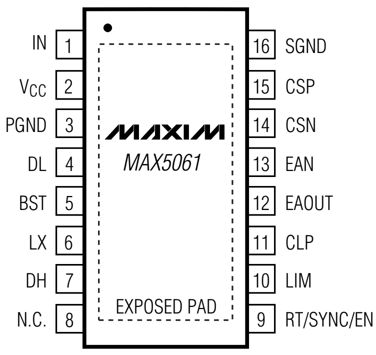
Use the following guidelines to layout the switching voltage regulator.

1) Place the IN, V_{CC}, and V_{DD} bypass capacitors close to the MAX5060/MAX5061.
2) Minimize the area and length of the high-current loops from the input capacitor, upper switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
3) Keep short the current loop formed by the lower switching MOSFET, inductor, and output capacitor.
4) Place the Schottky diodes close to the lower MOSFETs and on the same side of the PC board.
5) Keep the SGND and PGND isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
6) Run the current-sense lines CSP and CSN very close to each other to minimize the loop area. Similarly, run the remote voltage sense lines SENSE+ and SENSE- close to each other. Do not cross these critical signal lines through power circuitry. Sense the current right at the pads of the current-sense resistors.
7) Avoid long traces between the V_{DD} (MAX5060)/V_{CC} (MAX5061) bypass capacitors, driver output of the MAX5060/MAX5061, MOSFET gates, and PGND. Minimize the loop formed by the V_{CC} bypass capacitors, bootstrap diode, bootstrap capacitor, MAX5060/MAX5061, and upper MOSFET gate.
8) Place the bank of output capacitors close to the load.
9) Distribute the power components evenly across the board for proper heat dissipation.
10) Provide enough copper area at and around the switching MOSFETs, inductor, and sense resistors to aid in thermal dissipation.
11) Use 4oz copper to keep the trace inductance and resistance to a minimum. Thin copper PC boards can compromise efficiency since high currents are involved in the application. Also, thicker copper conducts heat more effectively, thereby reducing thermal impedance.

Pin Configurations



THIN QFN



TSSOP

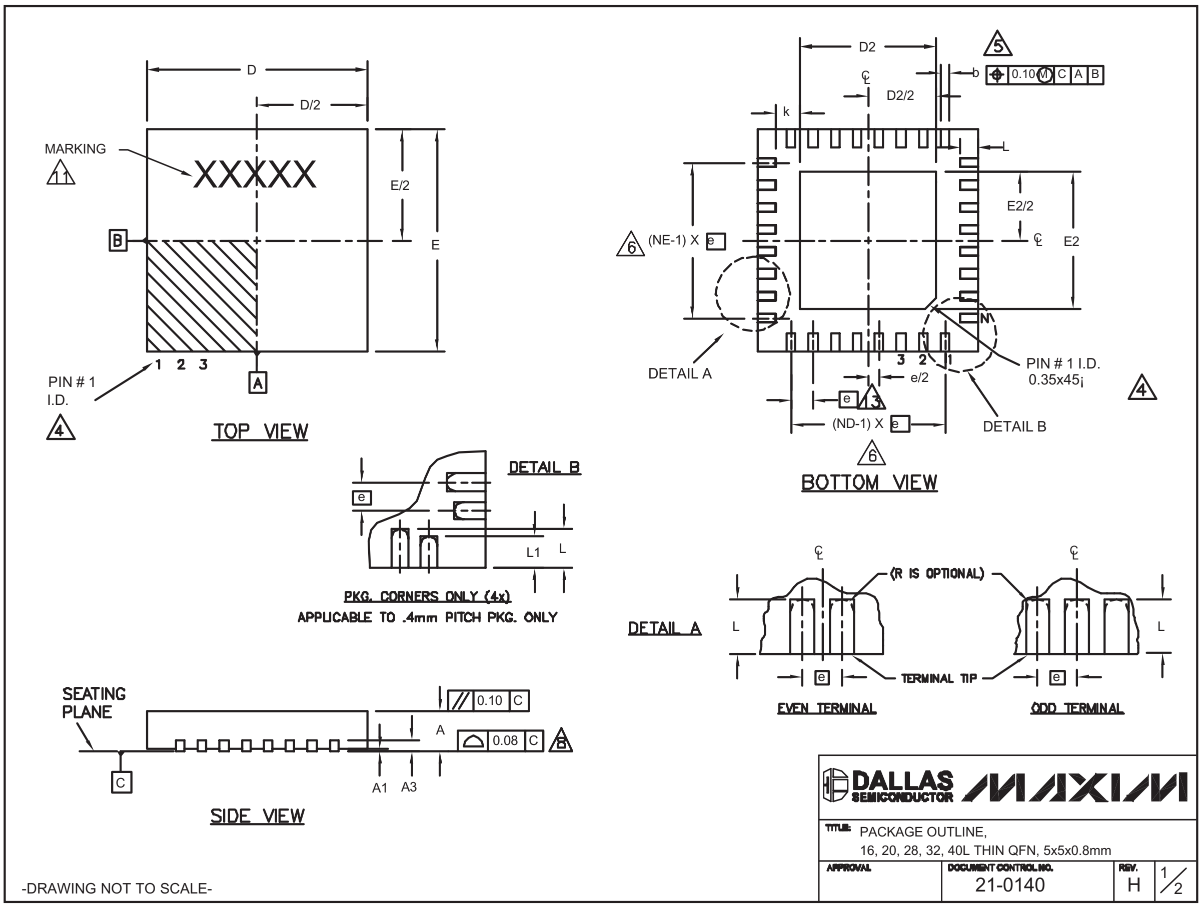
Chip Information

TRANSISTOR COUNT: 5654

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3, AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

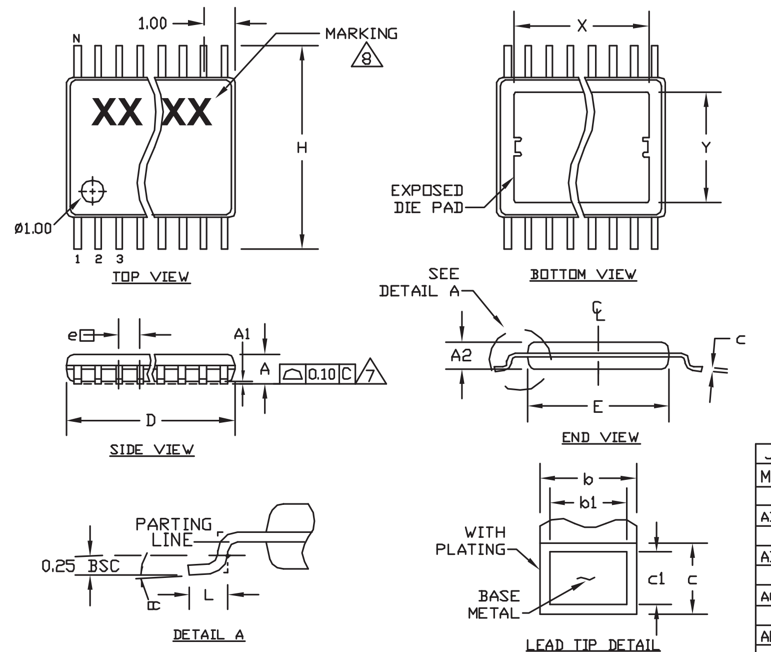
TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	H	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.00	0.15	0.000	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153, SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0108	E	1/1